Bachelor of Technology in Electronics Engineering (VLSI Design and Technology) (EE-VDT)

2nd Year Onward Scheme and implementation guideline

Third Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Theory Papers					
ES	ES-201	Computational Methods	4		4
HS/MS	HS-203	Indian Knowledge System*	2		2
PC	ECC-205	Signals and Systems	3		3
PC	ECC-207	Digital Logic and Computer Design	4		4
PC	ECC-209	Analog Communications	4		4
PC	ECC-211	Analog Electronics-I	4		4
Practical / Viva Voce					
ES	ES-251	Computational Methods Lab		2	1
PC	ECC-253	Digital Logic and Computer Design Lab		2	1
PC	ECC-255	Analog Communications Lab		2	1
PC	ECC-257	Analog Electronics-I Lab		2	1
PC	ECC-259	Signals and Systems Lab		2	1
Total			**21**	**10**	**26**

***NUES:**All examinations to be conducted by the concerned teacher as specified in the detailed syllabus of the paper.

Fourth Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Theory Papers					
BS	BS-202	Probability, Statistics and Linear Programming	4		4
HS/MS	HS-204	Technical Writing*	2		2
PC	EEC-206	Network Analysis and Synthesis	3		3
PC	ECC-210	Microprocessors and Microcontrollers	3		3
PC	ECC-212	Digital Communications	3		3
PC	ECC-214	Analog Electronics-II	3		3
PC	ECC-216	Electromagnetic Field Theory	3		3
Practical / Viva Voce					
BS	BS-252	Probability, Statistics and Linear Programming Lab		2	1
PC	ECC-256	Microprocessors and Microcontrollers Lab		2	1
PC	ECC-258	Digital Communications Lab		2	1
PC	ECC-260	Analog Electronics-II Lab		2	1
PC	EEC-262	Network Analysis and Synthesis Lab		2	1
Total			**21**	**10**	**26**

***NUES:**All examinations to be conducted by the concerned teacher as specified in the detailed syllabus of the paper.

Fifth Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Theory Papers					
HS/MS	HS-301	Economics for Engineers	2		2
PC	ECC-303	Digital Signal Processing	4		4
PC	ECC-305	Microelectronics	3		3
PC	EEC-307	Introduction to Control Systems	3		3
PC	ECC-309	Transmission Lines, Waveguides and Antenna Design	4		4
PC	ECC-311	Data Communication and Networking	4		4
Practical / Viva Voce					
PC	ECC-351	Digital Signal Processing Lab		2	1
PC	ECC-353	Microelectronics Lab		2	1
PC	EEC-355	Introduction to Control Systems Lab		2	1
PC	ECC-357	Transmission Lines, Waveguides and Antenna Design Lab		2	1
PC	ECC-359	Data Communication and Networking Lab		2	1
PC / Internship	ES-361	Summer Training Report - 1 *			1
Total			**20**	**10**	**26**

***NUES:**Comprehensive evaluation of the Summer Training Report – 1 (after 4th Semester) shall be done by the committee of teachers, constituted by the Academic Programme Committee, out of 100. The training shall be of 4 to 6 weeks duration. The training can be under the mentorship of a teacher of the institute.

Sixth Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Theory Papers					
HS/MS	MS-302	Principles of Management for Engineers	3		3
HS/MS	HS-304	Universal Human Values*	1		1
PC	ES-306T	Embedded System Architecture and Design	3		3
PC	ECE-306T	VHDL Programming	3		3
PC	VLSI-328T	Semiconductor Devices and Modelling	3		3
PC	VLSI-330T	VLSI	3		3
OAE		Open Area Elective Paper (OAE – 1)			4
Practical / Viva Voce					
PC	ES-306P	Embedded System Architecture and Design Lab		2	1
PC	ECE-306P	VHDL Programming Lab		2	1
PC	VLSI-328P	Semiconductor Devices and Modelling Lab		2	1
PC	VLSI-330P	VLSI Lab		2	1
HS/MS	HS-352	NSS / NCC / Cultural Clubs / Technical Society / Technical Club*			2
Total					**26**

***NUES:**All examinations to be conducted by the concerned teacher as specified in the detailed syllabus of the paper.

****NUES:** Comprehensive evaluation of the students by the concerned coordinator of NCC / NSS / Cultural Clubs / Technical Society / Technical Clubs, out of 100 as per the evaluation schemes worked out by these activity societies, organizations; the faculty co-ordinators shall be responsible for the evaluation of the same. These activities shall start from the 1st semester and the evaluation shall be conducted at the end of the 6th semester for students admitted in the first semester. Students admitted in the 2nd year (3rd semester) as lateral entry shall be evaluated on the basis their performance, by the faculty co-ordinator for the period of 3rd semester to 6th semester only.

Seventh Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Theory Papers					
HS/MS	MS-401	Principles of Entrepreneurship Mindset	2		2
PC	VLSI-443T	CMOS Analog Integrated Circuit Design	3		3
PC	VLSI-445T	CMOS Digital Circuits Design	3		3
PC	VLSI-449T	Low Power VLSI Design	3		3
PC	VLSI-451	VLSI Testing	4		4
OAE		Open Area Elective Paper (OAE – 2)			4
Practical / Viva Voce					
PC	VLSI-443P	CMOS Analog Integrated Circuit Design Lab		2	1
PC	VLSI-445P	CMOS Digital Circuits Design Lab		2	1
PC	VLSI-449P	Low Power VLSI Design Lab		2	1
PC / Project	ES-451	Minor Project**			3
PC / Internship	ES-453	Summer Training (after 6th semester) Report *			1
Total					**26**

***NUES:**Comprehensive evaluation of the Summer Training Report – 2 (after 6th Semester) shall be done by the committee of teachers, constituted by the Academic Programme Committee, out of 100. The training shall be of 4 to 6 weeks duration. The training can be under the mentorship of a teacher of the institute.

****The student shall be allocated a supervisor / guide for project work at the end 6th semester by the department / institution, the project shall continue into the 8th semester. In the 7th semester evaluation, the criteria for evaluation shall be conceptualization of the project work, the background study / literature survey and identification of objectives and methodology to be followed for project. 40 marks evaluation for the Teachers' Continuous Evaluation / Internal Assessment shall be done by concerned supervisor while the term end examination of 60 marks shall be conducted by the supervisor concerned and the external examiner deputed by the Examinations Division. In the absence of the supervisor, the Director of the Institution / Head of the Department can assign the responsibility of the supervisor (for purpose of examinations) to any faculty of the Institution / Department.

Eight Semester					
Group	**Paper Code**	**Paper**	**L**	**P**	**Credits**
Practical / Viva Voce%					
PC / Project	ES-452	Major Project – Dissertation and Viva Voce#			18
	ES-454	Project Progress Evaluation*			2
PC / Internship	ES-456	Internship Report and Viva Voce#			18
	ES-458	Internship Progress Evaluation*			2
Total			**0**	**0**	**20**

***NUES: Comprehensive evaluation by the committee of teachers, constituted by the Academic Programme Committee, out of 100.**

%By default every student shall do the project work (ES-452 and ES-454). A student shall either be allowed to do a project work (ES-452 and ES-454) or an internship (ES-456 and ES-458). The student must apply for approval to do internship before the commencement of the 8th semester to the institute, and only after approval of Principal / Director of the institute through Training and Placement Officer of the institute, shall proceed for internship.

#Students may be allowed to do internship in this semester in lieu of Major project. The students allowed to proceed for internship shall be required to maintain a log-book of activities performed during internship. The same has to be countersigned by the mentor at the organization where internship is completed.

ES-452: Evaluation shall be conducted of 40 marks (Teachers' continuous evaluation / internal assessment) by the supervisor. And, 60 marks by a bench of the supervisor and the external examiner deputed by Examination Division (COE), for a total of 100 marks.

ES-454 / ES-458: Comprehensive evaluation by the committee of teachers, constituted by the Academic Programme Committee, out of 100.

ES-456: Evaluation shall be conducted of 40 marks (Teachers' continuous evaluation / internal assessment) by the Training and Placement Officer of the department / institute on the basis of the report submitted by the student. And, 60 marks by a bench of the Training and Placement Officer of the department / institute and the external examiner deputed by Examination Division (COE), for a total of 100 marks.

In the absence of the supervisor or the Training and Placement Officer (as the case may be), the Director of the institute / Head of the Department can assign the responsibility of the supervisor or the Training and Placement Officer (for purpose of examinations) to any faculty of the department.

Note on Elective Papers: The elective papers shall be allowed to be taken / studied by the students, by the APC of the department / institute, keeping in view that two papers studied by the student should not have a substantial overlap. All papers studied by the student should be substantially distinct in content.

Note on Examination of Elective Papers:

(a) Papers with only theory component shall have 25 Marks continuous evaluation by the teacher and 75 Marks term-end examinations. Both these component marks shall be reflected on the marksheet of the student.
(b) Papers with only practical component shall have 40 Marks continuous evaluation by the teacher and 60 Marks term-end examinations. Both these component marks shall be reflected on the marksheet of the student.

Note on Continuous Evaluation of All Papers:

(a) Papers with only theory component shall have 25 Marks continuous evaluation by the teacher which shall be evaluated as:
   i. Mid-Term Test* - 15 Marks (after 8 weeks of teaching or as decided by PCC)
   ii. Assignments / Project / Quiz / Case Studies, etc. - 5 Marks
   iii. Attendance / Class Participation - 5 Marks
(b) Papers with only practical component shall have 40Marks continuous evaluation by the teacher which shall be evaluated as:
   i. Mid-Term Test and Viva Voce - 20 Marks (after 8 weeks of teaching or as decided by PCC)
   ii. Practical File - 10 Marks
   iii. Attendance / Lab Participation - 10 Marks

**** The mid-term test shall be coordinated by the Programme Coordination Committee.***

If a student could not appear for a mid-term test due to situation beyond the control by the student, a supplementary test may be arranged towards the end of the semester, in a similar manner to the mid-term test for such students. The students must apply for this provision to the department / institution. On examination of the reason for non-appearing in the mid-term test by the Head of the Department / Institute, and with reason for allowing to appear in the supplementary test to recorded by the Head of the Department / Institute, the student may be allowed.
The attendance sheets, the question papers and the award sheets for the continuous evaluation to be retained by the concerned department / institute for at least 6 months after the declaration of the result by the Examination Division of the University.

Open Area Electives

Semester	Paper Code	OAE – 1 (Choose Any One)	L	P	Credits
6	ES-304	Real Time Operating Systems	4		4
6	WMC-336T	Wireless Communication and Networks	3		3
	WMC-336P	Wireless Communication and Networks Lab		2	1
6	OCSE-306T	C++ Programming	3		3
	OCSE-306P	C++ Programming Lab		2	1
6	OCSE-342T	Programming in Java	3		3
	OCSE-342P	Programming in Java Lab		2	1
6	AI-316T	Artificial Intelligence and Machine Learning	3		3
	AI-316P	Artificial Intelligence and Machine Learning Lab		2	1
6	OSD-334T	Android App Development	3		3
	OSD-334P	Android App Development Lab		2	1
6	IPCV-334T	Digital Image Processing	3		3
	IPCV-334P	Digital Image Processing Lab		2	1
6	OUHV-338	Understanding Human Being, Nature and Existence Comprehensively	4		4
6	OUHV-340	Vision for Humane Society	4		4
6	CS-312T	Network Security and Cryptography	3		3
	CS-312P	Network Security and Cryptography Lab		2	1
6	IOT-324T	Introduction to Internet of Things	3		3
	IOT-324P	Introduction to Internet of Things Lab		2	1
6	IOT-326T	Introduction to Sensors and Transducers	3		3
	IOT-326P	Introduction to Sensors and Transducers Lab		2	1
6		MOOCs (Swayam / NPTEL)			4
Semester	**Paper Code**	**OAE – 2 (Choose Any One)**	**L**	**P**	**Credits**
7	WMC-453T	Ad hoc and Sensor Networks	3		3
	WMC-453P	Ad hoc and Sensor Networks Lab		2	1
7	ES-405T	Real Time Embedded System Programming	3		3
	ES-405P	Real Time Embedded System Programming Lab		2	1
7	FSD-435T	PHP Programming and MySQL	3		3
	FSD-435P	PHP Programming and MySQL Lab		2	1
7	MAC-409T	Robotics Engineering	3		3
	MAC-409P	Robotics Engineering Lab		2	1
7	OSD-445T	Data Structures and Algorithms	3		3
	OSD-445P	Data Structures and Algorithms Lab		2	1
7	OCSE-407T	Introduction to Database Management Systems	3		3
	OCSE-407P	Introduction to Database Management Systems Lab		2	1
7	SC-401T	Soft Computing	3		3
	SC-401P	Soft Computing Lab		2	1
7	DS-427T	Data Science using R	3		3
	DS-427P	Data Science using R Lab		2	1
7	IOT-441T	IoT with Arduino, ESP and Raspberry Pi	3		3
	IOT-441P	IoT with Arduino, ESP and Raspberry Pi Lab		2	1
7	NET-473T	Cloud Computing and Security	3		3
	NET-473P	Cloud Computing and Security Lab		2	1
7	OUHV-463	Holistic Human Health	4		4
7	FSD-437T	Mobile App Development	3		3
	FSD-437P	Mobile App Development Lab		2	1
7	IPCV-461T	Machine Learning for Image and Vision Analysis	3		3
	IPCV-461P	Machine Learning for Image and Vision Analysis Lab		2	1
7		MOOCs (Swayam / NPTEL)			4

Note:

1. Each OAE slot is of 4 credits, if in a particular slot, the paper has no practical component, then it is of 4 credits (a pure theory paper), otherwise for purpose of examination and conduct of classes, the course is split in two papers, namely a theory paper of 3 credits and a practical paper of 1 credit. The student has to study for 4 credits per slot of OAE group. This is reflected by suffixing the paper code by T (for Theory component) and P (for Practical component), if required

2. The Open Area Electives described / enumerated are the one offered by engineering departments. If other departments, offering minor specialization or elective papers as open area electives to engineering students (approved by the university Academic Council) are possible at the concerned institution, the same may also be offered to the engineering students studying in the major disciplines under the aegis of the University School of Information, Communication and Technology. The APC of the department / intuition shall allow the choice of such electives, provided they follow the credit framework of the programme of study for open area electives.

Implementation Rules:

1. ***The examinations, attendance criteria to appear in examinations, promotion and award of the degree shall be governed by the Ordinance 11 of the University.*** The term "major discipline" / "primary discipline" in this document refers to the discipline in which student is admitted / studies from 3rd semester onwards. However credits of courses / paper for OAE / EAE groups shall not be considered for the purpose of promotion from one year of study to the subsequent year of study.
2. ***Minimum duration*** of the Bachelor of Technology programme shall be 4 years (N=4 years) (8 semesters) for the students admitted in the 1st year and 1st semester of the degree programme. Lateral entry students shall be admitted in the 2nd year and 3rd semester of the degree programme (effectively in the batch admitted in the first year in the previous academic session and shall be deemed to have been exempted from the courses / papers of the first year of the degree programme. No exemption certificate shall be issued in any case.

   A specific lateral entry students' minimum duration shall be the same as the minimum duration for the batch in which he/she is admitted as a lateral entry student in the 2nd year.
3. ***Maximum duration of the Bachelor of Technology programme shall be 6 years (N+2 years).*** After completion of N+2 years of study, if the student has appeared in the papers of all the semesters upto 8th semester, then a maximum extension of 1 year may be given to the student for completing the requirements of the degree if and only if the number of credits already earned by the student is atleast 150 (for lateral entry students it shall be at least 102 credits) from the (non-honours components). Otherwise, the admission of the student shall stand cancelled. After the period of allowed study, the admission of the student shall be cancelled.

   A specific lateral entry students' maximum duration shall be the same as the minimum duration for the batch in which he/she is admitted as a lateral entry student in the 2nd year.
4. ***The degree shall be awarded only after the fulfilment of all requirements of the Scheme and Syllabus of Examinations and the applicable Ordinance.***
5. (a) The students shall undergo the following group of Courses / Papers as enumerated in the scheme (***For the students admitted in the First Year / First Semester).***

Group	Semester (Credits)							Total Credits	Mandatory Credits
	I & II	III	IV	V	VI	VII	VIII		
BS	24		5					**29**	**14**
HS/MS	6	2	2	2	6	2		**20**	**10**
ES	20	5						**25**	**15**
PC		19	19	24	16	20	20	**118**	**104**
OAE					4	4		**8**	**4**
Total	**50**	**26**	**26**	**26**	**26**	**26**	**20**	**200**	**147**

TABLE 1: Distribution of Credits (Project / Internship credits are 25 out the 118 credits for Programme Core (PC) credits, while extra-curricular activities credits are 2 out of 20 credits for Humanities / Management / Social Science Group (HS/MS)) . This table is for students admitted in the First Year / First Semester of the Degree Programme.

(b) The students admitted as Lateral Entry shall undergo the following group of Courses / Papers as enumerated in the scheme***.***

Group	Semester (Credits)						Total Credits	Mandatory Credits
	III	IV	V	VI	VII	VIII		
BS		5					**5**	**0**
HS/MS	2	2	2	6	2		**14**	**7**
ES	5						**5**	**0**
PC	19	19	24	16	20	20	**118**	**104**
OAE				4	4		**8**	**4**
Total	**26**	**26**	**26**	**26**	**26**	**20**	**150**	**115**

TABLE 2: Distribution of Credits (Project / Internship credits are 25 out the 118 credits for Programme Core (PC) credits, while extra-curricular activities credits are 2 out of 14 credits for Humanities / Management / Social Science Group (HS/MS)) This table is for students admitted as Lateral Entry Students in the Second Year / Third Semester of the Degree Programme.

6. Mandatory Credits specify the number of credits from each subject group to be mandatorily acquired by the student for the award of the degree,for students admitted as students in the 1st year and 1st semester of the degree programme. While for students admitted as lateral entry in the 2nd year and 3rd semester the Mandatory Credits value is 115, and specify the number of credits from each subject group to be mandatorily acquired by the student for the award of the degree (Table 2). See clause 11 and 12 also**.**

7. Some of the papers are droppable in the sense that the student may qualify for the award of the degree even when the student has not cleared / passed some of the papers of these group. However, the student has to earn the minimum credits for the programme of study as specified. **See clause 11 and 12 also**.

8. The students may take 2 subjects from OAE group. The open electives of the OAE group of courses may also be taken through SWAYAM / NPTEL MOOCs platform. The student desirous of doing a MOOC based course among the OAE group must seek approval of the APC of the institute for the same before the commencement of the semester. The APC shall allow the MOOC based OAE option to the student if and only if the MOOC subject / course being considered for the student is being offered in line with the Academic Calendar applicable. The student shall submit the successful completion certificate with marks to the institution for onwards transfer to the Examination Division. The Examinations Division shall take these marks on record for incorporation in the result of the appropriate semester. These marks / grades of these courses shall be used for calculation of the SGPA/CGPA of the student concerned by the examination division of the University. The degree to the student on fulfilment of other requirements for such cases shall be through **clause 12.a. or 12.b.**

   These MOOC courses taken by the students, if allowed by the APC of the institute shall be of 4 credits or more collectively to be against or for one paper slot in the scheme, through MOOCs, though the marks shall be shown individually. That is in one paper slot in the scheme wherever a MOOC course is allowed, the student may register for more than one paper to aggregate 4 credits or more. **If the credits of these MOOC Courses, allowed to a student is more than 4, then the maximum credit for the programme shall be amended accordingly for the particular student.** Also, in a particular semester, a student may take more than one MOOC course with the approval of the APC to meet the credit requirements of OAE for the semester. The cost of taking the MOOC course is to be borne by the concerned student. The results of the MOOC courses shall be declared separately by the Examination Division from the result for the papers conducted by the examination division of the University.

   No minor specialization shall be offered / awarded.

9. To earn an Honours degree, the student may enrol for 20 credits or more through SWAYAM / NPTEL MOOCs platform. This point has to be read together with other points specially point 13 and 14. The acquisition of the credits should be completed before the 15th of the July of the Admission Year plus 4 years. That is, if a student is admitted in the year X, then these credits must be acquired through MOOCs by 15th July of the

year (X+4), no extra duration or time shall be allocated, this means, the student must submit the result of such papers on or before 15th July of the Admission Year plus 4 years.

Honours in the degree shall be awarded if and only if at least 20 credits are acquired through MOOCs. To obtain Honours in the programme, the student must apply to the institution about the same before the commencement of the 5th semester. The specific courses through MOOCs shall be registered by the student only after approval by the Academic Programme Committee (APC) of the Institute. The APC shall approve the course if it is not already studied by the student or the student shall not study it in future and adds value to the major area of specialization (which is the degree). The papers for which the student desires to appear for Honours through MOOCs, all papers results shall be submitted by the student to the Institute for onwards transfer to Examination Division of the University, to be taken on record of the University. The results of these papers shall be a part of the records of the examinations of the students. The records shall be submitted by the student to the Institute, then transferred to the Examination Division, shall be notified by the Examination Division of the University, and a separate marksheet shall be issued by the Examination Division. The cost of taking the MOOC course is to be borne by the concerned student. Such courses shall be reflected as additional courses / papers for the student.

If a student acquires less than 20 credits through MOOCs, following the mechanism specified, then also the results of these papers shall be taken on record as specified above, though no Honours degree shall be awarded.

The papers through MOOCs for Honours degree shall not be a part of the set of the papers over which the SGPA / CGPA of the student shall be calculated.

The papers through MOOCs for Honours degree shall be additional papers studied by the students and are to be taken into account only for award of Honours in the degree programme, if 20 credits are earned through MOOCs as approved by APC, by a student. **See Clause 13 also.**

10. Maximum Credits is at least 200 (Table 1) for students admitted in the 1st year and 1st semester, these are the credits for which the student shall have to study for the non-Honours component of the curriculum. And, for lateral entry students admitted in the 2nd year and 3rd semester of the degree programme, the maximum credit required to be studied is at least 150 (Table 2). **See clause 8 also**.

    The student has to appear in the examinations for these credits in all components of evaluation as specified in the scheme of studies.

11. Minimum Credits required to be earned is atleast 180 (out of the 200 non Honours papers credits, see clause 10 also) for students admitted in the 1st year and 1st semester. And, for lateral entry students admitted in the 2nd year and 3rd semester of the degree programme, the minimum credit required to be earned Is at least 135 (out of the 150 non Honours papers credits, see clause 10 also). See clause 6 also.

12. The following degree route can be taken by a student **(also refer point 13)**:

    a. The students shall be awarded the degree without any minor specialization under the following conditions:

        i. The student has earned the mandatory credits as defined in **Table 1** or **Table 2** (as applicable) and **clause 6**.

        ii. In addition, the total credits (including the above specified credits) earned by the student is atleast as specified in **clause 11**.

    The degree nomenclature of the degree shall be as: "***Bachelor of Technology in Electronics Engineering (VLSI Design and Technology)";*** if criteria / **point 9** is not satisfied for Honours. Otherwise, if criteria / **point 9** is met, then the degrees shall be an Honours degree and the nomenclature shall be as: "***Bachelor of Technology in Electronics Engineering (VLSI Design and Technology) (Honours)***", if in addition to **point 12.b.i and 12.b.ii**, the student fulfils the criteria for Honours as specified at **point 9**.

    b. If the student does not fulfil any of the above criterions (**point 12.a, or 12.b**), if the student earns at least the minimum credits specified in clause 11 (disregarding the mandatory credits clause of **Table 1 or Table 2 (as applicable)** and **Clause 6**), then the student shall be award the degree as "***Bachelor of Technology in Electronics Engineering (VLSI Design and Technology)".*** Such students shall not be

eligible for the award of an Honours degree. Though, if credits are accumulated through MOOCs as per **clause 9**, the same shall be reflected in the marksheets of the students.

13. ***The Honours degree shall only be awarded if the CGPA of the student is above or equal to 7.5 in addition to fulfilment of criteria / point 10 and 13 above and the degree is awarded after the immediate completion of the 4th year of the batch from the year of admission.*** No Honours shall be conferred if the degree requirements are not completed in the minimum duration.
14. ***Pass marks in every paper shall be 40.***
15. ***Grading System shall be as per Ordinance 11 of the University.***
16. The institution shall offer atleast two elective groups out of the open area for students of each major discipline. The institute shall decide the group(s) and/or individual papers to be offered as electives based on the availability of infrastructure and faculty. From the groups / papers offered by the institute, an elective paper / group shall be taught if and only if the number of students in a paper is at-least 20 or at-least 1/3 of the students of a major discipline for which the paper / group is to be offered. The APC of the department / institute may define a maximum number of students allowed to register for a paper as an open area elective.
17. Teachers of the other department(s), as and when deputed by their department, for teaching the students enrolled in programmes offered by the department offering the programme shall be a part of the Academic Programme Committee of the discipline. Such teachers, for all academic matters, including teaching, teachers' continuous evaluation, term end examinations etc. shall be governed by the decisions of the APC of department offering the programme of study. Similarly, the guest faculty, the visiting faculty and the Contract / Ad Hoc faculty as and when deputed to teach students of a particular department shall form a part of APC of the department.
18. The Paper IDs will be generated / issued / assigned by the Examination Division of the University.
19. **The medium of instructions shall be English.**

Paper Code(s): ES-201	**L**	**P**	**C**
Paper: Computational Methods	**4**	**-**	**4**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To understand numerical methods to find roots of functions and first order unconstrained minimization of functions.
2.	To introduce concept of interpolation methods and numerical integration.
3.	To understand numerical methods to solve systems of algebraic equations and curve fitting by splines.
4.	To understand numerical methods for the solution of Ordinary and partial differential equations.

Course Outcomes (CO)

CO 1	Ability to develop mathematical models of low level engineering problems
CO 2	Ability to apply interpolation methods and numerical integration.
CO 3	Ability to solve simultaneous linear equations and curve fitting by splines
CO 4	Ability to numerically solve ordinary differential equations that are initial value or boundary value problems

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	2	2	2	2	-	-	-	2	2	2	3
CO 2	3	2	2	2	2	-	-	-	2	2	2	3
CO 3	3	3	3	3	2	-	-	-	2	2	2	3
CO 4	3	3	3	3	2	-	-	-	2	2	2	3

UNIT-I

Review of Taylor Series, Rolle 's Theorem and Mean Value Theorem, Approximations and Errors in numerical computations, Data representation and computer arithmetic, Loss of significance in computation
Location of roots of equation: Bisection method (convergence analysis and implementation), Newton Method (convergence analysis and implementation), Secant Method (convergence analysis and implementation). Unconstrained one variable function minimization by Fibonacci search, Golden Section Search and Newton's method. Multivariate function minimization by the method of steepest descent, Nelder- Mead Algorithm.

UNIT-II

Interpolation: Assumptions for interpolation, errors in polynomial interpolation, Finite differences, Gregory-Newton's Forward Interpolation, Gregory-Newton's backward Interpolation, Lagrange's Interpolation, Newton's divided difference interpolation
Numerical Integration: Definite Integral, Newton-Cote's Quadrature formula, Trapezoidal Rule, Simpson's one-third rule, simpson's three-eight rule, Errors in quadrature formulae, Romberg's Algorithm, Gaussian Quadrature formula.

UNIT-III

System of Linear Algebraic Equations: Existence of solution, Gauss elimination method and its computational effort, concept of Pivoting, Gauss Jordan method and its computational effort, Triangular Matrix factorization methods: Dolittle algorithm, Crout's Algorithm, Cholesky method, Eigen value problem: Power method Approximation by Spline Function: First-Degree and second degree Splines, Natural Cubic Splines, B Splines, Interpolation and Approximation

UNIT - IV

Numerical solution of ordinary Differential Equations: Picard's method, Taylor series method, Euler's and Runge-Kutta's methods, Predictor-corrector methods: Euler's method, Adams-Bashforth method, Milne's method.
Numerical Solution of Partial Differential equations: Parabolic, Hyperbolic, and elliptic equations
Implementation to be done in C/C++

Textbook(s):
1. E. Ward Cheney & David R. Kincaid , "Numerical Mathematics and Computing" Cengage; 7th ed (2013).

References:
1. R. L. Burden and J. D. Faires, "Numerical Analysis", CENGAGE Learning Custom Publishing; 10th Edition (2015).
2. S. D. Conte and C. de Boor, "Elementary Numerical Analysis: An Algorithmic Approach", McGraw Hill, 3rd ed. (2005).
3. H. M. Antia, "Numerical Methods for Scientists & Engineers", Hindustan Book Agency, (2002).
4. E Balagurusamy "Numerical Methods" McGraw Hill Education (2017).

Paper Code(s): HS-203	**L**	**P**	**C**
Paper: Indian Knowledge System	**2**	**-**	**2**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks
3. This is an NUES paper, hence all examinations to be conducted by the concerned teacher.

Instruction for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To understand the Indian knowledge System.
2.	To understand the foundational concepts for science and technology.
3.	To understand the ancient Indian mathematics and astronomy.
4.	To understand the ancient Indian engineering and technology.

Course Outcomes (CO)

CO 1	Ability to understand the Indian knowledge System.
CO 2	Ability to understand and apply foundational concepts for science and technology.
CO 3	Ability to understand and apply ancient Indian mathematics and astronomy
CO 4	Ability to understand ancient Indian engineering and technology.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	-	-	-	-	-	3	-	-	-	-	-	2
CO 2	-	-	-	-	-	3	-	-	-	2	-	2
CO 3	3	3	-	-	-	-	-	-	-	-	-	2
CO 4	3	3	-	-	-	-	-	-	-	-	-	2

UNIT-I

Indian Knowledge System (IKS) - An Introduction:
Overview of IKS - Importance of Ancient Knowledge; Defining IKS; The IKS Corpus – A Classification Framework; Chaturdaśa-Vidyāsthāna; History of IKS, Some unique aspects of IKS;
The Vedic Corpus – Introduction to Vedas; The Four Vedas and their divisions; Vedāngas; Vedic Life;
Philosophical Systems – Indian Philosophical Systems; Vedic Schools of Philosophy; Non-Vedic Philosophical Systems; Wisdom through the Ages – Purānas, Itihāsa as source of wisdom, Rāmāyana, Mahābhārata, Niti-śāstras, Subhāssitas.

UNIT-II

Foundational Concepts for Science and Technology:
Linguistics - Components of Language; Pānini's work on Sanskrit Grammar; Phonetics in Sanskrit; Patterns in Sanskrit Vocabulary; Computational Concepts in Astādhyāyi, Logic for Sentence Construction; Importance of Verbs; Role of Sanskrit in Natural Language Processing

Number System and Units of Measurement – Number System in India; Salient Features of the Indian Numeral System; Unique approaches to represent numbers; Measurements for Time, Distance and Weight; Pingala and the Binary System
Knowledge: Framework and Classification – The Knowledge Triangle; Prameya; Pramāna; Samśaya; Framework for establishing Valid Knowledge

UNIT-III

Mathematic and Astronomy in IKS:
Mathematics – Unique aspects of Indian Mathematics; Great Mathematicians and their Contributions; Arithmetic; Geometry; Trigonometry; Algebra; Binary Mathematics and Combinatorial Problems in Chandah-śāstra of Pingala, Magic Squares in India
Astronomy - Unique aspects of Indian Astronomy; Historical Development of Astronomy in India; The Celestial Coordinate System; Elements of the Indian Calendar; Āryabhatiya and the Siddhāntic Tradition; Pancānga; Astronomical Instruments; Jantar Mantar of Rājā Jai Singh Sawai

UNIT - IV

Engineering and Technology in IKS:
Engineering and Technology: Metals and Metalworking – The Indian S & T Heritage; Mining and Ore Extraction; Metals and Metalworking Technology; Iron and Steel in India; Lost wax casting of Idols and Artefacts; Apparatuses used for Extraction of Metallic Components
Engineering and Technology: Other Applications – Literary sources for Science and Technology; Physical Structures in India; Irrigation and Water Management; Dyes and Painting Technology; Surgical Techniques; Shipbuilding; Sixty-four Art Forums; Status of Indigenous S & T

Textbook(s):
1. B. Mahadevan, Vinayaka Rajat Bhat & Nagendra Pavana R.N., "Introduction to Knowledge System: Concepts and Applications" PHI (2022).

References:
1. C.M Neelakandhan & K.A. Ravindran, "Vedic Texts and The Knowledge Systems of India", Sri Sankaracharya University of Sanskrit, Kalady (2010).
2. P.P. Divakaran, "The Mathematics of India: Concepts, Methods, Connections", Springer (2018)
3. C.A. Sharma, "Critical Survey of Indian Philosophy", Motilal Banarasidass Publication (1964)
4. G. Huet, A. Kulkarni & P. Scharf, "Sanskrit Computational Linguistics", Springer (2009).
5. A.K. Bag, "History of Technology in India", Indian National Science Academy, Vol 1, (1997)

Paper Code(s): ECC-205	**L**	**P**	**C**
Paper: Signals and Systems	**3**	**-**	**3**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1.	To impart understanding about various types of signals and systems, their classifications, analysis and operations.
2.	To impart knowledge of use of transforms in analysis of signals and system.
3.	To impart skill to carry out simulation on signals and systems for observing effects of applying various properties and operations.
4.	To impart strong foundation of communication and signal processing to be studied in the subsequent semester

Course Outcome (CO):

CO 1	Ability to understand about various types of signals and systems, classify them, analyze them, and perform various operations on them.
CO 2	Ability to understand use of transforms in analysis of signals and system.
CO 3	Ability to carry out simulation on signals and systems for observing effects of applying various properties and operations.
CO 4	Ability to create strong foundation of communication and signal processing to be studied in the subsequently.

Course Outcomes (CO) to Programme Outcomes (PO) Mapping (Scale - 1: Low, 2: medium, 3: High)

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	-	-	-	1	1	1	1
CO 2	3	3	3	3	2	-	-	-	1	1	1	1
CO 3	3	3	3	3	2	-	-	-	1	1	1	1
CO 4	3	3	3	3	2	-	-	-	1	1	1	1

Unit I

Continuous and discrete time signals: Classification of Signals – Periodic aperiodic even – odd – energy and power signals – Deterministic and random signals – complex exponential and sinusoidal signals – periodicity – properties of discrete time complex exponential unit impulse – unit step impulse functions – Transformation in independent variable of signals: time scaling, time shifting. Determination of Fourier series representation of continuous time and discrete time periodic signals – Explanation of properties of continuous time and discrete time Fourier series. Representation of continuous time signals by its sample - Sampling theorem – Reconstruction of a Signal from its samples, aliasing – discrete time processing of continuous time signals, sampling of band pass signals.

Unit II

Continuous time Fourier Transform and Laplace Transform analysis with examples – properties of the Continuous-time Fourier Transform and Laplace Transform basic properties, Parseval's relation, and convolution in time and frequency domains.
Basic properties of continuous time systems: Linearity, Causality, time invariance, stability, magnitude and Phase representations of frequency response of LTI systems -Analysis and characterization of LTI systems using Differential Equations and Continuous time LTI systems. Laplace transform: Computation of impulse response and transfer function using Laplace transform.

Unit III

Discrete time system analysis using Difference equations, Discrete Time Fourier Transform, Discrete Fourier Transform, FFT and their property and usage in the analysis of Discrete time systems.

Unit IV

Basic principles of z-transform - z-transform definition – region of convergence – properties of ROC – Properties of z-transform – Poles and Zeros – inverse z-transform using Contour integration - Residue Theorem, Power Series expansion and Partial fraction expansion, Relationship between z-transform and Fourier transform. Properties of convolution and the interconnection of LTI Systems – Causality and stability of LTI Systems. Computation of Impulse & response & Transfer function using Z Transform.

Textbook(s):

1. Alan V. Oppenheim, Alan S. Willsky with S. Hamid Nawab, "Signals & Systems", 2nd ed., Pearson Education, 1997.
2. Simon Haykin and Barry Van Veen, "Signals and Systems", John Wiley, 1999

References:

1. M. J. Roberts, "Signals and Systems Analysis using Transform method and MATLAB", TMH 2003.
2. K. Lindner, "Signals and Systems", McGraw Hill International, 1999.
3. Moman .H. Hays," Digital Signal Processing ", Schaum's outlines, Tata McGraw-Hill Co Ltd., 2004.
4. B. P. Lathi, "Signal Processing and Linear System", Berkeley Cambridge Press, 1998.
5. H. P. Hsu, "Schaum's Outlines of The Theory and Problems of Signals and Systems", McGraw-Hill, 1995.
6. John G.Proakis and Dimitris G.Manolakis, "Digital Signal Processing, Principles, Algorithms and Applications, 3rd edn., PHI, 2000.

Paper Code(s): ECC-207	**L**	**P**	**C**
Paper: Digital Logic and Computer Design	**4**	**-**	**4**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To introduce basic concepts of Boolean Algebra and Combinational Logic
2.	To introduce various sequential circuits, designing with examples
3.	To relate combination circuit design and sequential circuit design with respect to the design of a computer system
4.	To introduce machine learning, computer arithmetic, modes of data transfer with respect to I/O and Memory organization of a computer

Course Outcomes (CO) :

CO 1	Ability to understand Boolean Algebra and Design Combinational Circuits .
CO 2	Ability to understand and Design Sequential Circuits.
CO 3	Ability to understand Design of a basic computer.
CO 4	Ability to understand Input-Output and Memory Organization of a Computer.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	2	3	2	2	-	-	-	3	2	2	3
CO 2	3	2	3	2	2	-	-	-	3	2	2	3
CO 3	3	2	3	3	2	-	-	-	3	2	2	3
CO 4	3	3	3	3	3	-	-	-	3	2	2	3

UNIT – I

Boolean Algebra and Combinational Logic: Review of number systems , signed, unsigned, fixed point, floating point numbers, Binary Codes, Boolean algebra – basic postulates, theorems , Simplification of Boolean function using Karnaugh map and Quine-McCluskey method – Implementations of combinational logic functions using gates, Adders, Subtractors, Magnitude comparator, encoder and decoders, multiplexers, code converters , parity generator/checker, implementation of combinational circuits using multiplexers.

UNIT – II

Sequential Circuits: General model of sequential circuits, Flip-flops, latches , level triggering, edge triggering, master slave configuration , concept of state diagram , state table, state reduction procedures , Design of synchronous sequential circuits , up/down and modulus counters , shift registers, Ring counter , Johnson counter , timing diagram , serial adder , sequence detector, Programmable Logic Array (PLA), Programmable Array Logic (PAL), Memory Unit, Random Access Memory

UNIT – III

Basic Computer organization: Stored Program, Organization, Computer registers, bus system, instruction set completeness, instruction cycle, Register Transfer Language, Arithmetic, Logic and Shift Micro-operations, Instruction Codes, Design of a simple computer, Design of Arithmetic Logic unit, shifter, Design of a simple hardwired control unit, Programming the basic computer, Machine language instructions, assembly language, Microprogrammed control, Horizontal and Vertical Microprogramming, Central Processing Unit, instruction sets and formats, addressing modes, data paths, RISC and CISC characteristics.

UNIT – IV

Computer Arithmetic, addition, subtraction, multiplication and division algorithms, Input-Output Organization, Modes of data transfer, Interrupt cycle, direct memory access, Input-Output processor, Memory Organization, Memory Hierarchy, Associative Memory, Cache Memory, Internal and external Memory, Virtual Memory.

Text Book(s)

1. M. Morris Mano, "Digital Logic and Computer Design", Pearson Education, 2016
2. M. Morris Mano, Rajib Mall "Computer System Architecture", 3rd Edition Pearson Education, 2017

References:

1. Leach, D. P., Albert P. Malvino, "Digital Principles and Applications", McGraw Hill Education, 8th Edition , 2014
2. Jain, R.P. ,"Modern Digital Electronics", McGraw Hill Education, 4th Edition , 2010
3. Floyd, Thomas L. , "Digital Fundamentals" Pearson Education, 11th Edition, 2017
4. M. Rafiquzzaman, "Fundamentals of Digital Logic and Microcomputer Design", Wiley, 5th Ed., 2005.

Paper Code(s): ECC-209	**L**	**P**	**C**
Paper: Analog Communication	**4**	**-**	**4**

Marking Scheme:
1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1.	To impart understanding of the concepts of analog communication systems.
2.	To impart understanding of various modulation and demodulation techniques of analog communication.
3.	To impart understanding of transmitters and receivers in analog communication.
4.	To impart understanding of the causes of noise and noise performance of analog communication.

Course Outcome (CO):

CO 1	To understand the concepts of analog communication systems.
CO 2	To understand various modulation and demodulation techniques of analog communication.
CO 3	To understand transmitters and receivers in analog communication.
CO 4	To understand the causes of noise and noise performance of analog communication.

Course Outcomes (CO) to Programme Outcomes (PO) Mapping (Scale - 1: Low, 2: medium, 3: High)

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT I

The Communication Process, Review of Fourier Transforms and Dirac Delta Functions, Transmission through Linear Systems, Filters (low pass and band pass signals), Phase and Group Delay, Sources of Information.
Amplitude Modulation: Introduction, Double Sideband – Suppressed Carrier Modulation, Quadrature – Carrier Multiplexing, Single-Sideband and Vestigial-Sideband methods of modulation, Frequency Translation, Frequency-Division Multiplexing

UNIT II

Angle Modulation: Introduction, Basic Definitions, Frequency Modulation, Phase-Locked Loop, Nonlinear Effects in FM Systems, Superheterodyne receiver.

UNIT III

Probability and Random Processes: Introduction; Probability; Random Variables, Statistical Averages; Random Processes; Mean, Correlation, and Covariance functions; Transmission of a Random Process Through a Linear Filter, Power Spectral Density, Gaussian Process, Noise, Narrowband Noise

UNIT IV

Noise: Introduction, Receiver Model, Noise in DSB-SC Receivers, Noise in AM Receivers, Noise in FM Receivers, Pre-emphasis and De-emphasis in FM.

Textbook(s):

1. Simon Haykins and Michael Moher, "Communication Systems" John Wiley &sons Inc, 5th edition, 2009.

References:

1. B P Lathi and Zhi Ding, "Modern Digital and Analog Communication Systems", OUP, 5th edition, 2019.
2. H. Taub, D. L. Schilling and Gaotam Saha, "Taub's Principles of Communication Systems", McGraw Hill Eduction, 4th edition, 2017.
3. J. G. Proakis, M. Salehi, "Fundamentals of Communications Systems", Pearson, 2nd Edition, 2014.
4. W. Tomasi, "Electronic communications systems (Fundamentals Through Advanced)", Pearson Education, 5th Edition, 2008.
5. G. Kennedy and B. Davis, "Electronic communication systems", TMH, 4th Edition, 2008 (reprint)

Paper Code(s): ECC-211	**L**	**P**	**C**
Paper: Analog Electronics – I	**4**	**-**	**4**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1.	To develop understanding of operation, characteristics, parameters and applications of p-n junction diode
2.	To develop understanding about BJT and FET in terms of structure, operation, configurations and characteristics. Also analyse stability and amplifier circuit using small signal models
3.	To impart knowledge of cascade amplifiers, coupling schemes, power amplifiers and their analysis
4.	To impart knowledge of Feedback amplifiers and oscillators

Course Outcome (CO):

CO 1	Ability to understand of operation, characteristics, parameters and applications of p-n junction diode
CO 2	Ability to understand about BJT and FET in terms of structure, operation, configurations and characteristics and able to analyse stability and amplifier circuit using small signal models
CO 3	Ability to understand and analyse cascade amplifiers, coupling schemes in amplifiers and power amplifiers
CO 4	Ability to understand feedback amplifiers and oscillators

Course Outcomes (CO) to Programme Outcomes (PO) Mapping (Scale - 1: Low, 2: medium, 3: High)

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT – I

Open circuit P-N junction diode, Forward and reverse biased diode, I-V characteristics of diode, Diode Equation, Temperature dependence of diode. Breakdown phenomena, diffusion and transition capacitance of diode. Diode equivalent circuit, Ideal diode. Solar cell.
Diode circuits: half-wave and full-wave rectifiers with capacitor filter, clamping and clipping circuits. Zener diodes as voltage regulator.

UNIT – II

Bipolar Junction transistor (BJT): Structure, modes of operation, Configurations, I-V characteristics, early effect, junction voltages; Transistor Biasing: Need of biasing, load line concept, fixed bias, self-bias, collector to base bias, stability factors, Current Mirrors; hybrid model of BJT amplifier, small signal analysis of CE BJT amplifier using h parameter
JFET: Physical structure, I-V characteristics; MOSFET: Depletion and enhancement types, Physical structure and I-V characteristics; FET small-signal model (low & high frequency); MOSFET as resistance and switch,

UNIT – III

Cascade amplifiers: Analysis of cascade amplifier (voltage gain, current gain, input and output impedances); Darlington pair, Cascode amplifier; Types of coupling: DC, RC and Transformer; RC coupled Amplifier and its frequency response; Differential Amplifier: differential and Common mode operation, CMRR.
Power Amplifiers: Classification of output stages (Class A, B, C & AB), Class A Amplifier, Transformer coupled class A amplifier, Push pull amplifiers: Class A and Class B, Harmonic distortion, efficiency, crossover distortion, class AB operation, Class C amplifier.

UNIT – IV

Feedback Amplifiers: classification, Feedback concept, basic feedback topologies, Characteristics of Negative Feedback, Feedback and stability, gain margin, Noise margin,
Sinusoidal Oscillator, Barkhausen criterion, RC phase shift, LC (Colpitt's, Hartley, Clapp), Crystal Oscillator.

Textbook(s):

1. J. Millman, C.C. Halkias and Satyabrata Jit, "Electronic Devices and Circuits", Tata McGraw Hill, 4th ed. , 1998
2. R. L. Boylestad and N. Nashlesky, "Electronic Devices and Circuit Theory", Pearson Education, 11th Ed., 2014

References:

1. Adel S. Sedra and Kenneth C. Smith, "Micro Electronic Circuits Theory and Applications," 5th Edition , OUP, 2004.
2. B. Kumar and S. B. Jain, "Electronic Devices and Circuits"", Prentice Hall of India, 2007
3. S Salivahanan, and N. Suresh Kumar, "Electronic Devices and Circuits", McGraw Hill Education (India), 2018
4. B.P. Singh and Rekha Singh, "Electronic Devices and Integrated Circuits", Pearson Education, 2009.
5. J. J. Cathey, "Schaum's Outline of Theory and Problems in Electronic Devices and Circuits", McGraw Hill, 2002.

Paper Code(s): ES-251	**L**	**P**	**C**
Paper: Computational Methods Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Computational Methods) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

Implementation to be done in C/C++

1. Program for finding roots of f(x)=0 Newton Raphson method.
2. Program for finding roots of f(x)=0 by bisection method.
3. Program for finding roots of f(x)=0 by secant method.
4. To implement Langrange's Interpolation formula.
5. To implement Newton's Divided Difference formula.
6. Program for solving numerical integration by Trapezoidal rule
7. Program for solving numerical integration by Simpson's 1/3 rule
8. To implement Numerical Integration Simpson 3/8 rule.
9. Inverse of a system of linear equations using Gauss-Jordan method.
10. Find the Eigen values using Power method.
11. Program for solving ordinary differential equation by Runge-Kutta Method.

Paper Code(s): ECC-253	**L**	**P**	**C**
Paper: Digital Logic and Computer Design Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Digital Logic and Computer Design) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Design and implementation of adders and subtractors using logic gates.
2. Design and implementation of 4-bit binary adder/subtractor.
3. Design and implementation of multiplexer and demultiplexer.
4. Design and implementation of encoder and decoder.
5. Construction and verification of 4-bit ripple counter and Mod-10/Mod-12 ripple counter.
6. Design and implementation of 3-bit synchronous up/down counter.
7. Design and computer architecture: Design a processor with minimum number of instructions, so that it can do the basic arithmetic and logic operations.
8. Write an assembly language code in GNUsim8085 to implement data transfer instruction.
9. Write an assembly language code in GNUsim8085 to store numbers in reverse order in memory location.
10. Write an assembly language code in GNUsim8085 to implement arithmetic instruction.
11. Write an assembly language code in GNUsim8085 to add two 8 bit numbers.
12. Write an assembly language code in GNUsim8085 to find the factorial of a number.
13. Write an assembly language code in GNUsim8085 to implement logical instructions.
14. Write an assembly language code in GNUsim8085 to implement stack and branch instructions.

Paper Code(s): ECC-255	**L**	**P**	**C**
Paper: Analog Communications Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Analog Communications) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Generation of DSB-SC AM signal using balanced modulator.
2. To study amplitude demodulation by linear diode detector
3. Generation of SSB AM signal.
4. To study envelop detector for demodulation of AM signal and observe diagonal peak clipping effect.
5. To generate FM signal using voltage controlled oscillator.
6. To generate a FM Signal using Varactor & reactance modulation.
7. Detection of FM Signal using PLL & foster seelay method.
8. To study Super heterodyne AM receiver and measurement of receiver parameters viz.sensitivity, selectivity & fidelity.
9. To study Pre-emphasis and De-emphasis in FM.
10. Generation of Phase modulated and demodulated signal.

Paper Code(s): ECC-257	**L**	**P**	**C**
Paper: Analog Electronics – I Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Analog Electronics - I) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To plot V-I characteristics of a semiconductor diode & Calculate Static & Dynamic Resistance.
2. To Study the Reverse characteristics of Zener diode
3. To Study the Rectifier circuit (With and Without Filter).
    a. Half Wave Rectifier
    b. Centre Tapped Rectifier.
    c. Bridge Rectifier.
4. Plotting input and output characteristics and calculation of parameters of a transistor in common emitter configuration.
5. Transistor biasing circuit. Measurement of operating point (Ic and Vce) for a :-
    a. fixed bias circuit
    b. potential divider biasing circuit.
6. Plot the FET characteristics & MOSFET characteristics.
7. To measure the overall gain of two stages at 1 KHz and compare it with gain of Ist stage, Also to observe the loading effect of second stage on the first stage
8. To plot the frequency response curve of two stage amplifier.
9. To study Emitter follower circuit & measurement of voltage gain and plotting of frequency response Curve.
10. Feedback in Amplifier. Single stage amplifier with and without bypass capacitor, measurement of voltage gain and plotting the frequency response in both cases.
11. To determine and plot firing characteristics of SCR by varying anode to cathode voltage, and varying gate current.
12. To note the wave shapes and voltages at various points of a UJT relaxation oscillator circuit.
13. For Transistorized push pull amplifier Measurement of optimum load, maximum undistorted power (by giving maximum allowable signal) Efficiency and percentage distortion factor.
14. To study the characteristics of single tuned & double tuned amplifier.

Paper Code(s): ECC-259	**L**	**P**	**C**
Paper: Signals and Systems Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Signals and Systems) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Introduction to MATLAB and its basic commands.
2. Plot unit step, unit impulse, unit ramp, exponential, parabolic functions and sinusoidal signals
3. Plot the linear convolution of two sequences.
4. Plot the correlation of two sequences.
5. Plot the magnitude and phase spectra of a signal using Fourier transforms.
6. Plot the magnitude and phase spectrum of signal using Fourier series.
7. Find out the Z transform of a signal and check the stability using pole zero location.
8. Plot the spectra of ideally sampled signal w.r.t. sampling of Discrete time signals.
9. Verification of few properties of Fourier transform.
10. Evaluate the DTFS coefficients of a signal and plot them.
11. Plot the step response for any impulse response entered by user.

Paper Code(s): BS-202	L	P	C
Paper: Probability, Statistics and Linear Programming	4	-	4

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1:	To understand probability and probability distributions.
2:	To understand methods of summarization of data.
3:	To understand and use test for hypothesis.
4:	To understand methods for solving linear programming problems.

Course Outcomes (CO):

CO1:	Ability to solve probability problems and describe probability distributions.
CO2:	Ability to describe and summarize data.
CO3:	Ability to use test for hypothesis.
CO4:	Ability to formulate and solve linear programming problems.

Course Outcomes (CO to Programme Outcomes (PO) Mapping (scale 1: low, 2: Medium, 3: High

CO/PO	*PO01*	*PO02*	*PO03*	*PO04*	*PO05*	*PO06*	*PO07*	*PO08*	*PO09*	*PO10*	*PO11*	*PO12*
CO1	-	3	1	1	1	-	-	-	-	-	1	2
CO2	-	3	1	1	1	-	-	-	-	-	1	2
CO3	-	3	2	2	1	-	-	-	-	-	2	2
CO4	-	3	3	3	1	-	-	-	-	-	2	2

Unit I

Basics: Probability and Statistical models, Sample Spaces and Events, Counting Techniques, Interpretations and Axioms of Probability, Unions of Events and Addition Rules, Conditional Probability, Intersections of Events and Multiplication and Total Probability Rules, Independence, Bayes' Theorem, Random Variables.
Discrete and Continuous Random Variables and Distributions: Probability Distributions and Probability Mass / density Functions, Cumulative Distribution Functions, Mean and Variance of a Random Variable, Discrete and continuous Uniform Distribution, Binomial Distribution, Geometric and Negative Binomial Distributions, Hypergeometric Distribution, Poisson Distribution. Normal Distribution, Normal Approximation to the Binomial, and Poisson Distributions; Exponential Distribution, Erlang and Gamma Distributions, Weibull Distribution, Lognormal Distribution, Beta Distribution.

Unit II

Joint Probability Distributions for Two Random Variables, Conditional Probability Distributions and Independence, Joint Probability Distributions for Two Random Variables, Covariance and Correlation, Common Joint Distributions, Linear Functions of RandomVariables, General Functions of Random Variables, Moment-Generating Functions.
Numerical Summaries of Data, Stem-and-Leaf Diagrams, Frequency Distributions and Histograms, Box Plots, Time Sequence Plots, Scatter Diagrams, Probability Plots. Point Estimation, Sampling Distributions and the Central

Limit Theorem without proof, General Concepts of Point Estimation, Methods of Point Estimation, Statistical Intervals for a Single Sample.

Unit III

Hypotheses Testing for a SingleSample: Tests on the Mean of a Normal Distribution with Variance Known / Unknown, Tests on the Variance and Standard Deviationof a Normal Distribution, Tests on a Population Proportion, Testing for Goodness of Fit, Nonparametric tests (Signed, Wilcoxon), Similarly Statistical Inference forTwo Samples.
Regression and Correlation: Linear Regression, Least Squares Estimators, Hypotheses testing for simple linear regression, Confidence Intervals, Adequacy of model, Correlation, Transformed Variables, Logistic Regression. Similarly, for multiple linear regression including aspects of MLR.

Unit IV

Linear Programming: Introduction, formulation of problem, Graphical method, Canonical and Standard form of LPP, Simplex method, Duality concept, Dual simplex method, Transportation and Assignment problem.

Textbooks:
1. *Applied Statistics and Probability for Engineers* by Douglas G. Montgomery and Runger, Wiley, 2018
2. *Linear Programming* by G. Hadley, Narosa, 2002

References:
1. *Miller and Freund's Probability and Statistics for Engineers* by Richard A. Johnson, Pearson, 10th Ed., 2018.
2. *Probability & Statistics for Engineers & Scientists* by Ronald E. Walpole, Raymond H. Myers, Sharon L. Myers and Keying Ye, Pearson, 2016.
3. *Statistics and probability with applications for engineers and scientists using Minitab, R and JMP*, C. Gupta, Irwin Guttman, and Kalanka P. Jayalath, Wiley, 2020.
4. *Probability and Statistics for Engineering and the Sciences*, Jay Devore, Cengage Learning, 2014.
5. *Probability and Statistics in Emgineering*, William W. Hines, Douglas C. Montgomery, David M. Goldman, and Connie M. Borror, Wiley, 2003.
6. *Operations Research: An Introduction* by Hamdy A. Taha, Pearson, 10th Edition, 2016

Paper Code(s): HS-204	L	P	C
Paper: Technical Writing	2	-	2

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks
3. This is an NUES paper, hence all examinations to be conducted by the concerned teacher.

Instruction for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1:	To improve grammar and sentence structure and build vocabulary.
2:	To understand how to write different types of writings.
3:	To understand how to compose different types of business documents.
4:	To understand business ethics and develop soft skills.

Course Outcomes (CO):

CO1:	Ability to improve grammar and sentence structure and build vocabulary.
CO2:	Ability to write different types of writings with clarity.
CO3:	Ability to write different types of business documents.
CO4:	Ability to apply business ethics and enhance personality.

Course Outcomes (CO to Programme Outcomes (PO) Mapping (scale 1: low, 2: Medium, 3: High

CO/PO	*PO01*	*PO02*	*PO03*	*PO04*	*PO05*	*PO06*	*PO07*	*PO08*	*PO09*	*PO10*	*PO11*	*PO12*
CO1	-	-	-	-	-	1	-	-	-	3	-	-
CO2	-	-	-	-	-	1	-	-	-	3	-	-
CO3	-	-	-	-	-	1	-	-	-	3	-	-
CO4	-	-	-	-	-	1	-	3	-	3	-	-

Unit I

Grammar and Vocabulary--- Types of sentences (simple, complex and compound) and use of connectives in sentences, Subject-verb agreement, Comprehension, Synonyms and Antonyms, Homophones and Homonyms, Word Formation: Prefixes and Suffixes, Indianism, Misappropriation and Redundant Words, Question Tags and Short Responses.

Unit II

Writing Styles -- Expository, Explanatory, Descriptive, Argumentative and Narrative.
Precis writing, Visual Aids in Technical Writing, Plagiarism and Language Sensitivity in Technical Writing, Dialogue Writing, Proposals: Purpose and Types.

Unit III

Letters at the Workplace—letter writing: Request, Sales, Enquiry, Order and Complaint.
Job Application---Resume and Cover letter, Difference between Resume and CV, Preparation for Interview.
Meeting Documentation--- Notice, Memorandum, Circular, Agenda, Office Order and Minutes of meeting, Writing Instructions.

Unit IV

Ethics and Personality Development-----The Role of Ethics in Business Communication—Ethical Principles, Time Management, Self-Analysis through SWOT and JOHARI Window, Emotional Intelligence and Leadership Skills, Team Building, Career Planning, Self Esteem.

Textbook:

1. Meenakshi Raman and Sangeeta Sharma, Technical Communication: Principles and Practice, Oxford University Press, New Delhi (2015).

References:

1. Sanjay Kumar and Pushp Lata, Communication Skills, Oxford University Press, New Delhi (2015).
2. Herta A Murphy, Herbert W Hildebrandt, Jane P Thomas, Effective Business Communication, Tata McGraw-Hill, Hill Publishing Company Limited, Seventh Edition.

Paper Code(s): EEC-206	**L**	**P**	**C**
Paper: Network Analysis and Synthesis	**3**	**-**	**3**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1.	To understand the network theorem in AC circuit.
2.	To understand mathematical modelling of circuit.
3.	To understand two port parameter and transfer function.
4.	To understand realization of passive network and filter.

Course Outcome (CO):

CO 1	Ability to apply network theorems in AC circuit.
CO 2	Ability to determine transient respond of circuit.
CO 3	Ability to determine two port parameter of circuit.
CO 4	Ability to realize the circuit from their transfer function.

Course Outcomes (CO) to Programme Outcomes (PO) Mapping (Scale - 1: Low, 2: medium, 3: High)

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT-I

Application of Mesh current analysis, Node voltage analysis and Network theorems in AC circuits.
Graph theory: concept of tree, tie set matrix, cut set matrix and application to solve electric networks.

UNIT-II

Periodic waveforms and signal synthesis, properties and applications of Laplace transform of complex waveform. System modeling in terms of differential equations and transient response of R, L, C, series and parallel circuits for impulse, step, ramp, sinusoidal and exponential signals by classical method and using Laplace transform.

UNIT-III

Two port networks – Introduction of two port parameters and their interconversion, interconnection of two 2-port networks, open circuit and short circuit impedances and ABCD constants, relation between image impedances and short circuit and open circuit impedances. Network functions, their properties and concept of transform impedance, Hurwitz polynomial.

UNIT IV

Positive real function and synthesis of LC, RC, RL Networks in Foster's I and II, Cauer's I& II forms, Introduction of passive filter and their classification, frequency response, characteristic impedance of low pass, high pass, Band Pass and Band reject prototype section.

Textbook(s):

1. W H Hayt "Engineering Circuit Analysis" TMH Eighth Edition
2. Kuo, "Network analysis and synthesis" John Weily and Sons, 2nd Edition.

Reference Books:

1. S Salivahanan "Circuit Theory " Vikas Publishing House 1st Edition 2014
2. Van Valkenburg, " Network analysis" PHI, 2000.
3. Bhise, Chadda, Kulshreshtha, " Engineering network analysis and filter design" Umesh publication, 2000.
4. D. R. Choudhary, "Networks and Systems" New Age International, 1999
5. Allan H Robbins, W.C.Miller "Circuit Analysis theory and Practice"Cengage Learning Pub 5th Edition 2013
6. Bell "Electric Circuit" Oxford Publications 7th Edition.

Paper Code(s): ECC-210 / ECC-313	**L**	**P**	**C**
Paper: Microprocessors and Microcontrollers	**3**	**-**	**3**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1.	To impart knowledge about architecture and instruction set of 8085 microprocessor so that students can implement 8085 assembly language programs.
2.	To impart knowledge about architecture and instruction set of 8086 microprocessor so that students can implement 8086 assembly language programs.
3.	To impart knowledge about interfacing of 8255, 8254/8253, 8251, 8259 and I/O devices with 8086 microprocessor.
4.	To impart knowledge about architecture and operation of 8051 microcontroller and their interfacing with memory and I/O.

Course Outcome (CO):

CO 1	Ability to understand and distinguish the use of different 8085 instructions, timing diagram, addressing modes, interrupts and apply those instructions for implementing assembly language programs.
CO 2	Ability to analyse the timing diagrams, understand its instruction set, assess its memory organisation and will implement the assembly language programs , interfacing of memory with 8086 successfully
CO 3	Understand and realize the interfacing of 8255 (PPI), 8254/8255 (PIT), 8251 (USART), 8259 (PIC), 8279 (Keyboard and display), Sample and hold circuit, DAC/ADC, LCD & Stepper motor with 8086 microprocessor.
CO 4	Understand the architecture and operation of 8051 microcontroller and ability to use them for designing various applications based on 8051 by implementing the elaborate instruction set.

Course Outcomes (CO) to Programme Outcomes (PO) Mapping (Scale - 1: Low, 2: medium, 3: High)

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	2	-	1	1	-	-	-	-	1
CO 2	3	3	3	2	3	1	1	-		-		1
CO 3	3	3	3	2	3	1	1	-	1	-	-	1
CO 4	3	3	3	2	3	1	1	-	-	-	-	1

UNIT - I

Introduction to Microprocessor Systems: Architecture and PIN diagram of 8085, Timing Diagram, memory organization, addressing modes, interrupts. Assembly Language Programming.

UNIT – II

8086 Microprocessor: 8086 Architecture, difference between 8085 and 8086 architecture, generation of physical address, PIN diagram of 8086, Minimum Mode and Maximum mode, Bus cycle, Memory Organization, Memory

Interfacing, Addressing Modes, Assembler Directives, Instruction set of 8086, Assembly Language Programming, Hardware and Software Interrupts.

UNIT – III

Interfacing of 8086 with 8255, 8254/8253, 8251, 8259: Introduction, Generation of I/O Ports, Programmable Peripheral Interface (PPI)-Intel 8255, Sample-and-Hold Circuit and Multiplexer, Keyboard and Display Interface, Keyboard and Display Controller (8279), Programmable Interval timers (Intel 8253/8254), USART (8251), PIC (8259), DAC, ADC, LCD, Stepper Motor.

UNIT – IV

Overview of Microcontroller 8051: Introduction to 8051 Micro-controller, Architecture, Memory organization, Special function registers, Port Operation, Memory Interfacing, I/O Interfacing, Programming 8051 resources, interrupts, Programmer's model of 8051, Operand types, Operand addressing, Data transfer instructions, Arithmetic instructions, Logic instructions, Control transfer instructions, Timer & Counter Programming, Interrupt Programming.

Textbook(s):

1. Muhammad Ali Mazidi, "Microprocessors and Microcontrollers", Pearson, 2006
2. Douglas V Hall, "Microprocessors and Interfacing, Programming and Hardware" Tata McGraw Hill, 2006.
3. Ramesh Gaonkar, "MicroProcessor Architecture, Programming and Applications with the 8085", PHI

References:

1. Muhammad Ali Mazidi, Janice GillispieMazidi, Rolin D. MCKinlay "The 8051 Microcontroller and Embedded Systems",2nd Edition, Pearson Education 2008.
2. Kenneth J. Ayala, "The 8086 Microprocessor: Programming & Interfacing The PC", Delmar Publishers, 2007.
3. A K Ray, K M Bhurchandi, "Advanced Microprocessors and Peripherals", Tata McGraw Hill, 2007.
4. Vaneet Singh, Gurmeet Singh, "Microprocessor and Interfacing", Satya Prakashan, 2007.

Paper Code(s): ECC-212	**L**	**P**	**C**
Paper: Digital Communications	**3**	**-**	**3**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1.	To understand importance of information theory in digital communication and various PCM modulation.
2.	To understand the various basic concepts of digital communication.
3.	To understand the various digital Modulation-demodulation techniques
4.	To understand various coding in digital communications.

Course Outcome (CO):

CO 1	Ability to understand the need of digital communication and conversion of analog to digital signals.
CO 2	Ability to understand the effect of additive white Gaussian Noise on digital communication modulation techniques.
CO 3	Ability to analyse the effect of inter symbol interference as the source of channel impairment and the effect of multipath phenomenon.
CO 4	Ability to use and design communication systems for reliable communication

Course Outcomes (CO) to Programme Outcomes (PO) Mapping (Scale - 1: Low, 2: medium, 3: High)

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT I

Review of probability theory and Stochastic processes, Poisson and Gaussian Process, Noise, Narrowband Noise, Sinewave plus Narrowband Noise. Sampling Theory, PAM, Quantization characteristics, PCM, DPCM, Delta Modulation, Adaptive Delta Modulation, Line Codes.

UNIT II

AWGN Channel Signalling: Geometric Representation of Signals, Conversion of Continuous AWGN Channel to a vector channel: ASK, QASK, FSK, M-array FSK, BPSK, DPSK, DEPSK, QPSK, M-array PSK, QAM, MSK, GMSK, Coherent and non-coherent detection and other keying techniques.

UNIT III

Band Limited Channels: Error rate due to channel noise in a matched filer receiver, Intersymbol Interference, Signal Design for Zero ISI, Raised cosine and square root raised cosine spectrum, Eye pattern, Adaptive equalization, signalling over multiple baseband channel, Fading Channels: Propagation effects, Jakes Model,

Statistical Characteristics of wideband wireless channel, Diversity techniques, MIMO, MIMO Capacity for channel known at receiver, OFDM, Spread-spectrum signals.

UNIT IV

Information Theory: Entropy, Source Coding Theorem, Lossless data compression, Discrete Memoryless channel, Mutual Information, Channel Capacity, Channel Coding Theorem, Differential Entropy and Mutual Information for Continuous Random Ensembles, Information Capacity Law. Error Control Coding: Introduction, Error Control using forward correction, Linear Block Code, Cyclic Codes, Convolutional Codes.

Textbook(s):

1. Simon Haykins, "Digital Communication Systems" John Wiley, 2014

References:

1. Simon Haykins and Michael Moher, "Communication Systems" John Wiley &sons Inc, 5th edition, 2009.
2. B P Lathi and Zhi Ding, "Modern Digital and Analog Communication Systems", OUP, 5th edition, 2019
3. H P Hsu, Schaum Outline Series, Analog and Digital Communications, TMH 2006
4. J.G Proakis, Digital Communication, 4th Edition, Tata Mc Graw Hill Company, 2001.

Paper Code(s): ECC-214	**L**	**P**	**C**
Paper: Analog Electronics – II	**3**	**-**	**3**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives:

1.	To understand Basic building block and characteristic of Op-Amp
2.	To understand the frequency response and Configurations of Op-Amp
3.	To analyze and design linear, nonlinear and Oscillators circuits using Op-Amp
4.	To analyze and design active filters and to understand function of Op-Amp based special ICs

Course Outcome (CO):

CO 1	Ability to understand and use Op-Amps to design open-loop and closed loop configuration.
CO 2	Ability to analyse frequency response of and Op-Amp circuit.
CO 3	Ability to use Op-Amp in linear and non-linear applications.
CO 4	Ability to design Active Filters

Course Outcomes (CO) to Programme Outcomes (PO) Mapping (Scale - 1: Low, 2: medium, 3: High)

CO/PO	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT – I

The Operational Amplifiers: Block diagram representation of OP-AMP; Evolution of IC and types, Power supply for Op-Amp; The Ideal Op-Amp: schematic, characteristics, equivalent circuit, Ideal voltage transfer curve, typical IC 741 characteristics

Open Loop Op-Amp configurations: The differential amplifier, inverting amplifier, non-inverting amplifier

Closed loop Op-Amp configurations: inverting and non-inverting amplifiers, voltage followers, differential amplifiers, closed loop frequency response & circuit stability, single supply operation of OP-AMP, Inverting and Non-Inverting op-amp.

UNIT – II

The Practical Op-Amp: Input offset voltage, input bias current, input offset current, Total output offset voltage, thermal drift, error voltage, Supply voltage rejection ration (SVRR), CMRR

Frequency Response of An Op-Amp: Frequency response compensator networks, High frequency OP-AMP equivalent circuit, open loop voltage gain as a function of frequency, Slew rate, causes of slew rates and its effects in application.

UNIT – III

Linear applications of Op-Amps: Summing, scaling and averaging amplifier (inverting, non-inverting & differential configuration), voltage to current & current to voltage converters, Integrator, Differentiator,
Non-Linear applications of IC op-amps: Comparator, Zero crossing detector, Schmitt Trigger, Clipping & Clamping Circuits, Precision Rectifiers, sample and hold circuit
Oscillators: Principles & Types; Phase shift, Wein-bridge & quadrature. Square wave, triangular wave and saw tooth wave generators, voltage-controlled oscillator

UNIT – IV

Active Filters: Classification and frequency response of filters, response Advantages of active filters, characteristics of butter worth, chebyshev, first order and second order butter worth filters- low pass and high pass types. Band pass & band reject filters.
Specialised IC- The 555 Timer: functional diagram, Monostable and Astable multivibrators; PLL: Basic PLL principle, monolithic 565 PLL; Voltage Regulators, Three terminal IC voltage regulators(LM 317

Textbook(s):

1. Ramakant A. Gayakwad, “OP-AMP and Linear ICs”, 4th Edition, Prentice Hall / Pearson Education, 2001.
2. D. Roy Choudhary & S. B Jain, “Linear Integrated Circuit”, 2nd ed. New age publication.2018.

References:

1. Adel S. Sedra and Kenneth C. Smith, “Micro Electronic Circuits Theory and Applications,” 5th Edition , OUP, 2004.
2. David A. Bell, “Op-amp & Linear ICs”, Oxford, 2013.
3. James M. Fiore, “Op Amps & Linear Integrated Circuits Concepts & Applications”, Cengage, 2010.
4. J. Michel Jacob, “Applications and Design with Analog Integrated Circuits”, PHI, 2004.
5. R. L. Boylestad and N. Nashlesky, “Electronic Devices and Circuit Theory”, Pearson Education, 11th Ed., 2014
6. J. Millman, C. Halkias, and C. D. Parikh, “Millman’s Integrated Electronics: Analog and Digital circuits and system”, McGraw Hill Education, 2018.

Paper Code(s): ECC-213 / ECC-216	**L**	**P**	**C**
Paper: Electromagnetic Field Theory	**3**	**-**	**3**

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To impart the basic laws of electrostatics.
2.	To impart the knowledge of electromagnetics.
3.	To impart the knowledge of solution to real life plan wave problems for various boundary conditions.
4.	To impart the knowledge of characteristics and impudence transformation on high frequency transmission lines.

Course Outcomes (CO)

CO 1	Ability to understand the basic laws of electrostatics.
CO 2	To understand the basic laws of electromagnetics.
CO 3	Ability to provide solution of real life plan wave problems for various boundary conditions.
CO 4	To understand the characteristics and impudence transformation on high frequency transmission lines

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	**PO02**	**PO03**	**PO04**	**PO05**	**PO06**	**PO07**	**PO08**	**PO09**	**PO10**	**PO11**	**PO12**
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT I

Introduction: Review of scalar and vector field, Dot and Cross products, Coordinate Systems-Cartesian, cylindrical and spherical. Vector representation of surface, Physical interpretation of gradient divergence and curl, Transformation of vectors in different co-ordinate systems, dirac-delta function.

Electrostatics: Electric field due to point-charges, line charges and surface charges, Electrostatic potential, Solution of Laplace and Poisson's equation in one dimension, M-method of image applied to plain boundaries, field mapping and conformal transformation, Electric flux density, Boundary conditions. Capacitance: calculation of capacitance for simple rectangular, cylindrical and spherical geometries, Electrostatic energy. [T1,T2]

UNIT II

Magnetostatics : Magnetic Induction and Faraday's Law, Magnetic Flux Density, Magnetic Field Strength H, Ampere, Gauss Law in the Differential Vector Form, Permeability, Energy Stored in a Magnetic Field, Ampere's Law for a Current Element, Volume Distribution of Current , Ampere's Law Force Law, Magnetic Vector Potential, The Far Field of a Current Distribution, Maxwell's Equations: The Equation of Continuity for Time Varying Fields, Inconsistency of Ampere's Law, Maxwell's Equations, Conditions at a Boundary Surface.

[T1,T2]

UNIT III

Electromagnetic Waves: Continuity equations, Displacement current, Maxwell's equation, Boundary conditions, Plane wave equation and its solution in conducting and non-conducting media, Phasor notation, Phase velocity, Group velocity, Depth of penetration, Conductors and dielectrics, Impedance of conducting medium. Polarization, Reflection and refraction of plane waves at plane boundaries, Poynting vectors, and Poynting theorem.
[T1,T2]

UNIT IV

Transmission Lines: Transmission line equations, Characteristic impendence, Distortion-less lines, Input impendence of a loss less line, computation of primary and secondary constants, Open and Short circuited lines, Standing wave and reflection losses, Impedance matching, Loading of lines, Input impedance of transmission lines, RF lines, Relation between reflection coefficient and voltage standing wave ratio (VSWR), Lines of different lengths – λ/2, λ/4, λ/8 lines, Losses in transmission lines, Smith chart and applications, impedance matching Single stub, Double stub. [T1,T2]

Textbook(s):

1. Matthew N. O. Sadiku , "Elements of Electromagnetics", Oxford University Press
2. E. C. Jordon, K. G. Balman, "Electromagnetic Waves & Radiation System" PHI – 2nd Edition

Reference Books:

1. William H. Hayt, "Engineering Electromagnetics", TMH
2. J.D. Kraus, "Electromagnetics", TMH
3. David K. Cheng," Field and Wave Electromagnetic", 2nd Edition, Pearson Education Asia,2001
4. John R. Reitz, "Foundations of Electromagnetic Theory". Pearson

Paper Code(s): BS-252	**L**	**P**	**C**
Paper: Probability, Statistics and Linear Programming Lab	**-**	**2**	**1**

Marking Scheme:

1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:

1. The course objectives and course outcomes are identical to that of (Probability, Statistics and Linear Programming) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

Implementation to be done in MATLAB or in equivalent software.

1. Installation of Scilab and demonstration of simple programming concepts like marix multiplication (scalar and vector), loop, conditional statements and plotting.

2. Program for demonstration of theoretical probability limits.

3. Program to plot normal distributions and exponential distributions for various parametric values.

4. Fitting of binomial distributions for given n and p.

5. Fitting of binomial distributions after computing mean and variance.

6. Fitting of Poisson distributions for given value of lambda.

7. Fitting of Poisson distributions after computing mean.

8. Fitting of normal distribution when parameters are given.

9. Fitting of linear regression line through given data set and testing of goodness of fit using mean error.

10. Fitting of Multiple Linear Regression (MLR) curve through given data set and testing of goodness of fit using mean error.

11. Solve a LPP of three variable using Simplex Method.

12. Solve a Transportation problem of three variables.

13. Solve an Assignment problem of three variables.

Paper Code(s): ECC-256 / ECC-363	**L**	**P**	**C**
Paper: Microprocessors and Microcontrollers Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Microprocessors and Microcontrollers) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Write a program to add and subtract two 16-bit numbers with/ without carry using 8086.

2. Write a program to multiply two 8 bit numbers by repetitive addition method using 8086.

3. Write a Program to generate Fibonacci series.

4. Write a Program to generate Factorial of a number.

5. Write a Program to read 16-bit Data from a port and display the same in another port.

6. Write a Program to generate a square wave using 8254.

7. Write a Program to generate a square wave of 10 kHz using Timer 1 in mode 1(using 8051).

8. Write a Program to transfer data from external ROM to internal (using 8051).

9. Design a Minor project using 8086 Microprocessor (Ex: Traffic light controller/temperature controller etc)

10. Design a Minor project using 8051 Micro controller

Paper Code(s): ECC-258	**L**	**P**	**C**
Paper: Digital Communications Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Digital Communications) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To Study Sampling Theorem.
2. To Study Pulse Code Modulation.
3. To Study Differential Pulse Code Modulation.
4. To Study Delta Modulation.
5. To Study Adaptive Delta Modulation.
6. To Study Amplitude Shift Keying (ASK) and calculate its S/N ratio and Probability of error.
7. To Study Phase Shift Keying (PSK) and calculate its S/N ratio and Probability of error.
8. To Study frequency Shift Keying (FSK) and calculate its S/N ratio and Probability of error.
9. To Study Differential Phase Shift Keying Modulation (DPSK) and calculate its S/N ratio and Probability of error.
10. To Study Quadrature Phase Shift Keying Modulation (QPSK) and calculate its S/N ratio and Probability of error.
11. To Study Quadrature Amplitude Modulation (QAM) and calculate its S/N ratio and Probability of error.

Paper Code(s): ECC-260	**L**	**P**	**C**
Paper: Analog Electronics – II Lab	**-**	**2**	**1**

Marking Scheme:

1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:

1. The course objectives and course outcomes are identical to that of (Analog Electronics - II) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To study the op-amp (IC 741) as inverting and non-inverting amplifier and calculate its gain.
2. Observe and plot the output Wave shape of Op-Amp R-C differentiating circuits, R-C integrating circuits for square wave input
3. To study the op-amp (IC 741) as adder, subtractor and voltage follower, calculate its output voltage..
4. Construct biased and unbiased series and shunt clipping circuits & combinational clipper circuit for positive and negative peak clipping of a sine wave.
5. To study RC phase shift/Wien Bridge oscillator measurement of frequency and amplitude of oscillations using Op-Amp.
6. To study the waveform of square wave generator using 741 Op-Amp IC.
7. To study the waveform of Schmitt Trigger circuit & Precision Rectifier using 741 OP-AMP IC.
8. To make and test the operations of Monostable Multivibrator circuits using 555 timer.
9. To make and test the operations of Astable Multivibrator circuits using 555 timer.
10. To study the Sallen Key Voltage controlled voltage source active filters.

Paper Code(s): EEC-262	**L**	**P**	**C**
Paper: Network Analysis and Synthesis Lab	**-**	**2**	**1**

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Network Analysis and Synthesis) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Introduction to MATLAB and its basic commands.
2. Plot unit step, unit impulse, unit ramp, exponential, parabolic functions and sinusoidal signals
3. Study the transient response of series RLC circuit for different types of waveforms on CRO and verify using MATLAB
4. Study the time response of a simulated linear system and verify the unit step and square wave response of first order and second order, type 0,1 system
5. Using MATLAB determine current in various resistors connected in network using mesh current and node voltage analysis.
6. To determine Z and Y parameters of the given two port network.
7. To determine ABCD parameters of the given two port network.
8. To verify Reciprocity Theorem for the given two port network.
9. To determine Hybrid parameters of the given two port network.
10. To design Cascade Connection and determine ABCD parameters of the given two port network.
11. To design Series-Series Connection and determine Z parameters of the given two port network.
12. To design Parallel-Parallel Connection and determine Y parameters of the given two port network.
13. To design Series-Parallel Connection and determine h parameters of the given two port network
14. Study the frequency response of different filter circuits.

Economics for Engineers	L	P	C
	2		2

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
All	5	HS/MS	HS	HS-301

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To explain the basic micro and macro economics concepts.
2.	To analyze the theories of production, cost, profit and break even analysis.
3.	To evaluate the different market structures and their implications for thebehavior of the firm.
4.	To apply the basics of national income accounting and business cycles toIndian economy.

Course Outcomes (CO)

CO 1	Analyze the theories of demand, supply, elasticity and consumer choicein the market.
CO 2	Analyze the theories of production, cost, profit and break even analysis.
CO 3	Evaluate the different market structures and their implications for thebehavior of the firm.
CO 4	Apply the basics of national income accounting and business cycles toIndian economy.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	1	2	1	2	1	-	1	-	1	1	3	1
CO 2	1	2	1	2	1	-	1	-	1	1	3	1
CO 3	1	2	1	2	1	-	1	-	1	1	3	1
CO 4	1	2	1	2	1	-	1	-	1	1	3	1

UNIT-I

Introduction: Economics Definition, Basic economic problems, Resource constraints and welfare maximization. Microand Macro economics. Production Possibility Curve.Circular flow of economic activities.
Basics of Demand, Supply and Equilibrium: Demand side and supply side of the market. Factors affecting demand & supply. Elasticity of demand & supply – price, income and cross-price elasticity. Market equilibrium price.

UNIT-II

Theory of Consumer Choice: Theory of Utility and consumer's equilibrium.Indifference Curve analysis, Budget Constraints, Consumer Equilibrium.
Demand forecasting: Regression Technique, Time-series, Smoothing Techniques: Exponential, Moving AveragesMethod

UNIT-III

Cost Theory and Analysis: Nature and types of cost, Cost functions- short run and long run, Economies and diseconomies of scale
Market Structure: Market structure and degree of competitionPerfect competition, Monopoly, Monopolistic competition, Oligopoly

UNIT - IV

National Income Accounting: Overview of Macroeconomics, Basic concepts of NationalIncome Accounting
Macro Economics Issues: Introduction to Business Cycle, Inflation-causes,consequences and remedies: Monetary and Fiscal policy.

Textbook(s):
1. H.C. Petersen, W.C. Lewis, Managerial Economics, 4th ed., Pearson Education 2001.

References:
1. S.K. Misra& V. K. Puri, Indian Economy, 38th ed., Himalaya Publishing House, 2020.
2. D.N. Dwivedi, Managerial Economics, 8th Edition, Vikas Publishing house
3. D. Salvatore, Managerial Economics in a Global Economy, 8th ed., Oxford University Press, 2015.
4. S. Damodaran, Managerial Economics, 2 nd ed., Oxford University Press, 2010.
5. M. Hirschey, Managerial Economics, 12th ed., Cengage India, 2013.
6. P.A. Samuelson, W.D. Nordhaus, S. Nordhaus,Economics,18th ed., Tata Mc-Graw Hill, 2006.

Digital Signal Processing	L	P	C
	4		4

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/ICE/EE-VDT/EC-ACT	5	PC	PC	ECC-303

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To impart the basic knowledge of DFT, its properties, FFT and its applications.
2.	To impart the knowledge of designing and realization of FIR filters.
3.	To impart the knowledge of designing and realization of IIR filters.
4.	To impart the knowledge of quantization errors in Digital Signal Processing and the concept of Multirate signal processing.

Course Outcomes (CO)

CO 1	To understand the basic concept of DFT and FFT.
CO 2	To Acquire a clear idea of FIR filter designing techniques and realization methods.
CO 3	To understand the IIR filter designing techniques and realization methods and the stability.
CO 4	To understand the quantization errors in Digital Signal Processing and the concept of Multirate signal processing.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT I

Review of Discrete Time Fourier Transform, Z- transform and Discrete Fourier Transform, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs, concept of circular convolution, computation of circular convolution by graphical and matrix form, relationship between linear convolution and circular convolution, computation of linear convolution from circular convolution, , linear filtering using DFT, aliasing error, filtering of long data sequences – Overlap-Save and Overlap-Add methods
Efficient computation of the DFT: Complexity analysis of direct computation of DFT, Concept of Fast Fourier transformation, Radix-2 computation of FFT using decimation-in-time and decimation-in-frequency algorithms, signal flow graphs, Butterflies, computations of FFT in one place using both algorithms, bit-reversal process, examples for DIT & DIF FFT Butterfly computations

UNIT II

Design & structure of FIR filters: Characteristics of practical frequency-selective filters, Basic concepts of IIR and FIR filters, Gibbs Phenomenon, Symmetric and Anti-symmetric FIR filters, Design of Linear-phase FIR filters using windows- Rectangular, Hamming, Hanning, Bartlett windows, FIR differentiator, FIR Hilbert Transformer. Design of FIR filters using frequency sampling method. Structure for FIR Systems: Direct form, Cascade form and Lattice structures.

UNIT III

Design & Structure of IIR filters: Concept of IIR digital filter, recursive and non-recursive system analog to digital domain transformation- Approximation of derivatives ,impulse invariant method and bilinear transformation and their properties, limitations of bilinear transformation, frequency warping and prewarping, methods to find out the order of IIR filter, mapping of poles and zeroes of filter in analog domain, computation of filter transfer function in analog domain, digital filter realization techniques, procedure to design Butterworth and Chebyshev digital IIR filters. Direct, Cascade, Parallel , Signal Flow graph and transposed structure, Lattice structures, Lattice and Lattice-Ladder Structures, Schur - Cohn stability Test for IIR filters

UNIT IV

Quantization Errors in Digital Signal Processing: Fixed point and floating point representation of numbers, Errors resulting from Rounding and Truncation, Digital Quantization of filter coefficients, Round-off effects in digital filters, Dead Band Effects.
Multirate Digital Signal Processing: Decimation, Interpolation, Sampling rate conversion by a rational factor; Frequency domain characterization of Interpolator and Decimator; Polyphase decomposition, Applications of Multirate signal processing.

Textbook(s):
1. Oppenheim & Schafer, Digital Signal Processing, PHI-latest edition.
2. Proakis and Manolakis, Digital Signal Processing, PHI Publication

Reference Books:
1. S. K. Mitra, Digital Signal Processing, TMH edition2006
2. Johny. R. Johnson, Introduction to Digital Signal Processing, PHI, Latest edition
3. R.Babu, Digital Signal Processing, Scitech Publication.

Microelectronics	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-305

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To comprehend semiconductor physics, band theory, and material behavior, demonstrating knowledge of semiconductor applications in electronic devices.
2.	To analyze and design analog and digital circuits, exhibiting skills in circuit analysis techniques for complex electronic systems.
3.	To gain practical knowledge of semiconductor fabrication processes, understanding techniques such as lithography, doping, and their impact on device performance.
4.	To use microelectronic components in designing and prototyping electronic systems, integrating devices into applications like integrated circuits, sensors, and communication devices.

Course Outcomes (CO)

CO 1	Comprehend semiconductor physics, band theory, and material behavior, demonstrating knowledge of semiconductor applications in electronic devices.
CO 2	Ability to analyze and design analog and digital circuits, exhibiting skills in circuit analysis techniques for complex electronic systems.
CO 3	Gain practical knowledge of semiconductor fabrication processes, understanding techniques such as lithography, doping, and their impact on device performance.
CO 4	Ability to use microelectronic components in designing and prototyping electronic systems, integrating devices into applications like integrated circuits, sensors, and communication devices.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	2	2	1	1	-	-	2	1	2
CO 2	2	3	3	2	3	1	2	-	1	2	2	2
CO 3	2	3	3	2	3	1	2	-	1	2	2	2
CO 4	2	3	3	2	3	1	2	-	1	2	2	2

UNIT I

Introduction to Microelectronics, Overview of Microelectronics Technology, Basic IC Fabrication Processes (Oxidation, Diffusion, Ion Implantation, etc.), Cleanroom Protocols and Safety Measures. CMOS & NMOS process technology. MOS capacitor, device structure & electrical characteristics. MOS under external bias, derivation of threshold voltage equation, enhancement & depletion transistor, MOS device design equations, MOSFET capacitances. MOSFET scaling and various short channel effects, Moore's law, multi-gate MOSFETs, non-conventional MOSFET, technology nodes and ITRS.

UNIT II

CMOS inverter and its DC characteristics, Static & dynamic power dissipation. Rise time, fall time delays, noise margin. Combinational CMOS logic circuits, pass transistor and transmission gate designs, Sequential MOS logic circuits: SR latch, CMOS D latch and edge triggered flip flop. Dynamic CMOS logic circuits: Domino CMOS logic, NORA CMOS logic, Zipper, TSPC.

UNIT III

Current Mirrors and Differential Amplifiers, Operational Amplifiers (Op-Amps) Design: Ideal vs. Practical Models, Frequency Response of Op-Amps, Feedback Topologies (Voltage, Current, and Transconductance Feedback), Voltage Reference Circuits, Linear Voltage Regulators, Switching Voltage Regulators, Stability Analysis and Compensation Techniques.

Unit IV

Static RAM (SRAM) Design: 6T Cell, Read and Write Operations, Dynamic RAM (DRAM) Design: Basic Cell, Refresh Techniques, Flash Memories: NOR and NAND Architectures, Non-Volatile Memories Design: EEPROM, Ferroelectric RAM (FeRAM), MRAM, Low-Power IC Design Techniques, Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), Radio-Frequency Integrated Circuits (RFICs): Basics and Applications.

Textbooks:

1. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2016). Digital Integrated Circuits: A Design Perspective. Pearson.
2. Razavi, B. (2016). Design of Analog CMOS Integrated Circuits. McGraw-Hill Education.
3. Weste, N. H. E., & Harris, D. (2015). CMOS VLSI Design: A Circuits and Systems Perspective. Pearson.
4. Kang, S. M., & Leblebici, Y. (2016). CMOS Digital Integrated Circuits: Analysis and Design. McGraw-Hill Education.

References:

1. Gray, P. R., Hurst, P. J., Lewis, S. H., & Meyer, R. G. (2001). Analysis and Design of Analog Integrated Circuits. Wiley.
2. Malvino, A. P., & Bates, J. A. (2012). Electronic Principles. McGraw-Hill Education.
3. Sedra, A. S., & Smith, K. C. (2014). Microelectronic Circuits. Oxford University Press.
4. Lee, T. H. (2004). The Design of CMOS Radio-Frequency Integrated Circuits. Cambridge University Press.

Introduction to Control Systems	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE/EEE/ICE/EE-VDT/ EC-ACT	5	PC	PC	EEC-307

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To provide an understanding about the concepts of transfer unction and its evaluation.
2.	To expose the students to time response of control systems
3.	To understand the frequency response of control systems
4.	To study compensators and controllers

Course Outcomes (CO)

CO 1	Ability to define, understand various terms related to control system and evaluation of transfer function
CO 2	Ability to apply knowledge of various types of signals in time response of systems
CO 3	Ability to analyse frequency response of systems
CO 4	Ability to design compensators and controllers

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	2	1	1	1	1	-	1	3	-	3
CO 2	3	2	1	3	2	1	1	-	1	3	-	1
CO 3	3	2	1	2	3	1	1	-	1	3	-	3
CO 4	3	3	2	1	1	1	1	-	1	3	-	3

UNIT I

Control Systems: Basics & Components Introduction to basic terms, classifications & types of Control Systems, Mathematical modelling of real life systems, block diagrams & signal flow graphs. Transfer function, determination of transfer function using Block diagram reduction techniques and Mason's Gain formula. Control system components: Electrical/ Mechanical/Electromechanical/A.C./D.C. Servo Motors, Stepper Motors, Tacho Generators, Synchros, Magnetic Amplifiers, Servo Amplifiers.

UNIT II

Time: Domain Analysis of real life problems, Time domain performance specifications, transient response of first & second order systems, steady state errors and static error constants in unity feedback control systems, response with P, PI and PID controllers, limitations of time domain analysis.

UNIT III

Frequency Domain Analysis frequency domain specifications and performance of LTI systems, minimum/non minimum phase systems, Polar and inverse polar plots, Logarithmic plots (Bode plots), gain and phase margins, relative stability. Correlation with time domain performance, closed loop frequency responses from open loop response. Limitations of frequency domain analysis.

UNIT IV

Stability & Compensation Techniques Concepts, absolute, asymptotic, conditional and marginal stability, Routh–Hurwitz and Nyquist stability criterion, Root locus technique and its application. Concepts of compensation, series/parallel/ series-parallel/feedback compensation, Lag/Lead/Lag-Lead networks for compensation, compensation using P, PI, PID controllers.

Textbooks:

1. B. C. Kuo, “Automatic control system”, Prentice Hall of India, 7th edition 2001.
2. Nagrath Gopal, “Control Systems Engineering -Principles and Design” New Age Publishers

References:

1. Norman S. Nise, “Control systems engineering” John Wiley & Sons (Asia) Singapore.
2. B. S. Manke, Linear Control System, Khanna publication.
3. K. Ogata, “Modern control engineering”, Pearson 2002.
4. A. K. Jaurath , Problems And Solutions Of Control Systems: With Essential Theory (CBS Problems and Solutions Series)

Transmission Lines, Waveguides and Antenna Design	L	P	C
	4		4

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-309

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To familiarise the various types of transmission lines and to deliberate the losses associated.
2.	To communicate information about waveguide concepts
3.	To impart the understanding of characteristics of different types of high frequency resonators.
4.	To impart the knowledge to define different terminologies of antenna parameters.

Course Outcomes (CO)

CO 1	To Understand the primary model of wave propagation in Transmission Lines and Analyze the various line parameters and Apply smith chart for line parameter and impedance calculations.
CO 2	Discuss the fundamental concepts of wave propagation in rectangular and circular waveguides and evaluate their characteristics.
CO 3	Understand the characteristics of resonance frequency of different types of resonator and its modes configuration.
CO 4	To describe the basic parameters of antenna and interpret to solve the radiation components

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	1	-	2	1	-	2
CO 2	3	3	3	3	2	1	1	-	2	1	-	2
CO 3	3	3	3	3	2	1	1	-	2	1	-	2
CO 4	3	3	3	3	2	1	1	-	2	1	-	2

UNIT I

Microwave Transmission Lines: Transmission-Line Equations, Solutions of Transmission-Line Equations. Reflection Coefficient, Transmission Coefficient. Standing Wave, Standing-Wave Ratio, Line Impedance, Line Admittance, Open and short circuited lines. Smith Chart Impedance Matching: Single-Stub Matching, Double-Stub Matching. Losses in transmission lines. Lines of different lengths – λ/2, λ/4, λ/8 lines.
Introduction to Microstrip transmission line.

UNIT II

Microwave Waveguides and Components:

Introduction Rectangular Waveguides: Solutions of Wave Equations in Rectangular Coordinates, TE Modes in Rectangular Waveguides, TM Modes in Rectangular Waveguides, Power Transmission in Rectangular Waveguides, Losses in Rectangular Waveguides, Excitations of Modes in Rectangular Waveguides.
Circular Waveguides: Solutions of Wave Equations in Cylindrical Coordinates, TE Modes in Circular Waveguides, TM Modes in Circular Waveguides, Excitations of Modes in Circular Waveguides.

UNIT III

Microwave Resonators: Series and Parallel Resonant Circuits: Series Resonant Circuit, Parallel Resonant Circuit, Loaded and Unloaded *Q.*
Transmission Line Resonators: Short-Circuited λ/2 line, Open-Circuited λ/2, Short-Circuited λ/4 Line; Rectangular Waveguide Cavities: Resonant Frequencies, *Q* of the TE_{10l} Mode; Circular Waveguide Cavities: Resonant Frequencies, Q of the TE_{nml} Mode. Dielectric Resonators: Resonant Frequencies, *Q* of the $TE_{01\delta}$ Mode. Excitation of Resonators: Critical Coupling, A Gap-Coupled Microstrip Resonator.

UNIT IV

Antennas: Introduction, Types of Antennas, Radiation Mechanism. Introduction monopole and dipole antenna.
Fundamental Parameters: Introduction, Radiation Pattern, Radiation Power Density, Radiation Intensity, Beamwidth, Directivity, Antenna Efficiency, Gain, Realized Gain, Beam Efficiency, Antenna Radiation Efficiency, Friis Transmission Equation and Radar Range Equation
Radiation Integrals and Auxiliary Potential Functions: The Vector Potential A for an Electric Current Source J, The Vector Potential F for A Magnetic Current Source M, Electric and Magnetic Fields for Electric (J) and Magnetic (M) Current Sources, Solution of the Inhomogeneous Vector Potential Wave Equation, Far-Field Radiation, Duality Theorem, Reciprocity Theorems

Textbook(s):
1. M. N. O. Sadiku , “Elements of Electromagnetics”, Oxford University Press 2007
2. S.Y Liao, “Microwave devices and Circuits” Pearson publications
3. D.M Pozar, “Microwave Engineering”, Wiley Publications.
4. Antenna for all Application-John D Kraus, third edition-TMH publication
5. Antenna Theory-Constantine A. Balanis -Third edition-Wiley Publication

References:
1. E. C. Jordon, K. G. Balman, “Electromagnetic Waves & Radiation System” Prentice Hall, India
2. Antennas and Wave Propagation–G. S. N. Raju (Pearson)
3. Foundations of Antenna Theory and Techniques – Vincent F. Fusco(Pearson)

Data Communication and Networking	L	P	C
	4		4

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-311

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To build an understanding of the fundamental concepts of data communication.
2.	To familiarize the student with the basic taxonomy of data link layer.
3.	To understand and implements the network routing, IP addressing, subnetting.
4.	To enumerate the functions of transport layer and application layer.

Course Outcomes (CO)

CO 1	Understand basic concepts of data communications.
CO 2	Understand and explain various functions of data link layerr.
CO 3	Understand and implements the network routing, IP addressing, subnetting.
CO 4	Enumerate the functions of transport layer and application layer.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	2	1	1	3	1	-	-	-	-	-	3
CO 2	3	2	1	1	3	1	-	-	-	-	-	3
CO 3	3	2	1	1	3	1	-	-	-	-	-	3
CO 4	3	2	1	1	3	1	-	-	-	-	-	3

UNIT- I

Data Communications : Components, protocols and standards, Network and Protocol Architecture, Reference Model ISO-OSI, TCP/IP-Overview ,topology, transmission mode, digital signals, digital to digital encoding, digital data transmission, DTE-DCE interface, interface standards, modems, cable modem, transmission media-guided and unguided, transmission impairment, Performance, wavelength and Shannon capacity. Review of Error Detection and Correction codes.

Switching: Circuit switching (space-division, time division and space-time division), packet switching (virtual circuit and Datagram approach), message switching.

UNIT- II

Data Link Layer: Design issues, Data Link Control and Protocols: Flow and Error Control, Stop-and-wait ARQ. Sliding window protocol, Go-Back-N ARQ, Selective Repeat ARQ, HDLC, Point-to –Point Access: PPP Point –to-Point Protocol, PPP Stack

Medium Access Sub layer: Channel allocation problem, Controlled Access, Channelization, multiple access protocols, IEEE standard 802.3 & 802.11 for LANS and WLAN, high-speed LANs, Token ring, FDDI based LAN, Network Devices-repeaters, hubs, switches bridges.

UNIT- III

Network Layer: Design issues, Routing algorithms, Congestion control algorithms,
Host to Host Delivery: Internetworking, addressing and routing, IP addressing (class full & Classless), Subnet, Network Layer Protocols: ARP, IPV4, ICMP, IPV6 ad ICMPV6.

UNIT- IV

Transport Layer: Process to Process Delivery: UDP; TCP, congestion control and Quality of service.
Application Layer: Client Server Model, Socket Interface, Domain Name System (DNS): Electronic Mail (SMTP), file transfer (FTP), HTTP and WWW.

Text Books:

1. A. S. Tannenbum, D. Wetherall, "Computer Networks", Prentice Hall, Pearson, 5th Ed
2. Behrouz A. Forouzan, "Data Communications and Networking", Tata McGraw-Hill, 4th Ed

Reference Books:

1. Fred Halsall, "Computer Networks", Addison – Wesley Pub. Co. 1996.
2. Larry L, Peterson and Bruce S. Davie, "Computer Networks: A system Approach", Elsevier, 4th Ed
3. Tomasi, "Introduction To Data Communications & Networking", Pearson 7th impression 2011
4. William Stallings, "Data and Computer Communications", Prentice Hall, Imprint of Pearson, 9th Ed.
5. Zheng , "Network for Computer Scientists & Engineers", Oxford University Press
6. Data Communications and Networking: White, Cengage Learning

Digital Signal Processing Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/ICE/EE-VDT/EC-ACT	5	PC	PC	ECC-351

Marking Scheme:

1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:

1. The course objectives and course outcomes are identical to that of (Digital Signal Processing) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Write Program to compute N point DFT of a given sequence and to plot magnitude and phase spectrum.
2. To implement Parseval theorem of DFT
3. To implement Time shifting and time reversal property of DFT
4. To find linear convolution of two given sequences.
5. To find circular convolution of two given sequences
6. To perform linear convolution from circular convolution and vice versa
7. To design LP FIR filter using windowing techniques
8. To design HP FIR filter using windowing techniques
9. To design LP IIR Butterworth filter for given specifications
10. To design LP IIR Chebyshev type-1 filter for given specifications
11. To verify the decimation of a given sequence
12. To verify the interpolation of a given sequence

Microelectronics Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-353

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Microelectronics) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To study the MOS characteristics and introduction to tanner EDA software tools.
2. To design and study the DC characteristics of PMOS and NMOS.
3. To design and study the DC and AC characteristics of CMOS inverter.
4. To design and study the characteristics of CMOS NAND and NOR gate.
5. To design any Boolean function using transmission gates.
6. To design and study the characteristics of CMOS multiplexer.
7. To design and study the layout of PMOS and NMOS transistors.
8. To design and study the layout of CMOS inverter.
9. To design and study the layout of 2 I/P CMOS NAND gate
10. To design and study the layout of 2 I/P CMOS NOR gate
11. To design and study the layout of CMOS XOR gate.

Introduction to Control Systems Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE/EEE/ICE/EE-VDT/ EC-ACT	5	PC	PC	EEC-355

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Introduction to Control Systems) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Determination of step & impulse response for a second-order unity feedback system.
2. To study the speed-torque characteristics of SERVO MOTOR.
3. Experiment to draw synchro pair characteristics.
4. To determine the Transfer Function of the DC Machine.
5. Plot unit step response of the given transfer function and finds delay time, rise time, and peak overshoot.
6. Plot the pole-zero configuration in the s-plane for the given transfer function.
7. To determine the characteristics of Magnetic Amplifiers.
8. Linear System Analysis (Time Domain Analysis, Error Analysis) Using MATLAB.
9. To observe the effect of P, PI, PID, and PD Controller for open loop and closed loop of second order system.
10. To analyze the frequency response of a system by plotting Root locus, Bode plot, and Nyquist plot using MATLAB software.
11. Experiment to draw the frequency response characteristics of the lag–lead compensator network and determination of its transfer function.
12. Temperature Controller Using PID Controller.
13. Study of operation of a stepper motor interface with a microprocessor.

Transmission Lines, Waveguides and Antenna Design Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-357

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Transmission Lines, Waveguides and Antenna Design) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To design and simulate a coaxial transmission line and obtain the propagation constant.
2. To design and simulate strip line and microstrip line and coplanar line and obtain the propagation constants.
3. To design and simulate a rectangular waveguide.
4. To design and simulate a circular waveguide.
5. To design and simulate a dipole antenna.
6. To design and simulate a slotted a rectangular waveguide antenna.
7. To design and simulate a leaky wave antenna using the rectangular waveguide.
8. To design and simulate a rectangular microstrip patch antenna.
9. To design and simulate a circular patch antenna.
10. To design and simulate a rectangular microstrip patch antenna array.
11. To design and simulate a circular microstrip patch antenna array.

Note: These experiments may be performed using simulation software like HFSS, CST and IE3D.

Data Communication and Networking Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE/EE-VDT/EC-ACT	5	PC	PC	ECC-359

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Data Communication and Networking) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Introduction to Computer Network laboratory
   Introduction to Discrete Event Simulation
   Discrete Event Simulation Tools - ns2/ns3, Omnet++
2. Using Free Open Source Software tools for network simulation – I Preliminary usage of the tool ns3
   Simulate telnet and ftp between N sources - N sinks (N = 1, 2, 3). Evaluate the effect of increasing data rate on congestion.
3. Using Free Open Source Software tools for network simulation - II
   Advanced usage of the tool ns3
   Simulating the effect of queueing disciplines on network performance - Random Early Detection/Weighted RED / Adaptive RED (This can be used as a lead up to DiffServ / IntServ later).
4. Using Free Open Source Software tools for network simulation - III
   Advanced usage of the tool ns3 Simulate http, ftp and DBMS access in networks
5. Using Free Open Source Software tools for network simulation - IV
   Advanced usage of the tool ns3
   Effect of VLAN on network performance - multiple VLANs and single router.
6. Using Free Open Source Software tools for network simulation - IV
   Advanced usage of the tool ns3
   Effect of VLAN on network performance - multiple VLANs with separate multiple routers.
7. Using Free Open Source Software tools for network simulation - V
   Advanced usage of the tool ns3
   Simulating the effect of DiffServ / IntServ in routers on throughput enhancement.
8. Using Free Open Source Software tools for network simulation - VI
   Advanced usage of the tool ns3
   Simulating the performance of wireless networks
9. Case Study I : Evaluating the effect of Network Components on Network Performance
   To Design and Implement LAN With Various Topologies and To Evaluate Network Performance Parameters for DBMS etc)
10. Case Study II : Evaluating the effect of Network Components on Network Performance
    To Design and Implement LAN Using Switch/Hub/Router As Interconnecting Devices For Two Different LANs and To Evaluate Network Performance Parameters.
11. Mini project - one experiment to be styled as a project of duration 1 month (the last month)

Principles of Management for Engineers	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
All	6	HS/MS	MS	MS-302

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To describe the functions, roles and skills of managers and illustrate how the manager's job is evolving.
2.	To evaluate approaches to goal setting, planning and organizing in a variety of circumstances.
3.	To evaluate contemporary approaches for staffing and leading in an organization
4.	To analyze contemporary issues in controlling for measuring organizational performance.

Course Outcomes (CO)

CO 1	Examine the relevance of the political, legal, ethical, economic andcultural environments in global business
CO 2	Evaluate approaches to goal setting, planning and organizing in a variety of circumstances.
CO 3	Evaluate contemporary approaches for staffing and leading in an organization
CO 4	Analyze contemporary issues in controlling for measuring organizational performance.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	2	2	1	2	-	2	-	-	1	2	3	2
CO 2	2	2	1	2	-	2	-	-	1	2	3	2
CO 3	2	2	1	2	-	2	-	-	1	2	3	2
CO 4	2	2	1	2	-	2	-	-	1	2	3	2

UNIT-I

Introduction to Managers and Management: Management an Overview: Introduction, Definition ofManagement, Role of Management, Functions of Managers,Levels of Management, Management Skills andOrganizational Hierarchy, Social and EthicalResponsibilities of Management: Arguments for and againstSocial Responsibilities of Business, Social Stakeholders,Measuring Social Responsiveness and Managerial Ethics,Omnipotent and Symbolic View, Characteristics andimportance of organizational culture, Relevance of political,legal, economic and Cultural environments to globalbusiness, Structures and techniques organizations use asthey go international .

UNIT-II

Planning: Nature & Purpose, Steps involved in Planning, Objectives, Setting Objectives, Process of Managing by Objectives, Strategies, Policies & Planning Premises, CompetitorIntelligence, Benchmarking, Forecasting, Decision-Making.

Directing: Scope, Human Factors, Creativity and Innovation,Harmonizing Objectives, Leadership, Types of Leadership,Directing, Managers as leaders, Early LeadershipTheories…Trait Theories, Behavioral Theories, ManagerialGrid, Contingency Theories of Leadership, Directing ...PathGoal Theory, contemporary views of Leadership, CrossCultural Leadership, Leadership Training, Substitutes ofLeadership

UNIT-III

Organizing: Organizing ,Benefits and Limitations-De-Centralization andDelegation of Authority, Authority versus Power,Mechanistic Versus Organic Organization ,CommonOrganizational Designs, Contemporary OrganizationalDesigns and Contingency Factors, The LearningOrganization Nature and Purpose, Formal and InformalOrganization, Organization Chart, Structure and Process,Departmentalization by difference strategies, Line and Staffauthority- Benefits and Limitations-De-Centralization andDelegation of Authority Versus, Staffing,Human ResourceInventory, Job Analysis , Job Description, Recruitment and

UNIT - IV

Controlling: Controlling, Introduction to Controlling System and processof Controlling, Requirements for effective control, Theplanning Contol link, The process of control, types ofcontrol The Budget as Control Technique, InformationTechnology in Controlling, Productivity, Problems andManagement, Control of Overall Performance, Direct andPreventive Control, Financial Controls, Tools formeasuring organizational Performance, Contemporaryissues in control Workplace concerns, employee theft,employee violence

Textbook(s):

1. Tripathi PC. Principles of management. Tata McGraw-Hill Education; 6th Edition 2017.

References:

1. Koontz H, Weihrich H. Essentials of management: an international, innovation, and leadershipperspective. McGraw-Hill Education; 10th Edition 2018.
2. Principles of Management Text and Cases, Pravin Durai , Pearson ,2015
3. Robbins, S.P. &Decenzo, David A. Fundamentals of Management,7th ed., Pearson, 2010
4. Robbins, S.P. & Coulter, Mary Management; 14 ed.,Pearson , 2009

Universal Human Values	L	P	C
	1		1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
All	6	HS/MS	HS	HS-304

Marking Scheme:

4. Teachers Continuous Evaluation: 25 marks

5. Term end Theory Examinations: 75 marks

6. This is an NUES paper, hence all examinations to be conducted by the concerned teacher.

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper.

Course Objectives :

1.	To help the students appreciate the essential complementarily between 'VALUES' and 'SKILLS' to ensure sustained happiness and prosperity which are the core aspirations of all human beings.
2.	To facilitate the development of a Holistic perspective among students towards life and profession as well as towards happiness and prosperity based on a correct understanding of the Human reality and the rest of existence. Such a holistic perspective forms the basis of Universal Human Values and movement towards value-based living in a natural way.
3.	To highlight plausible implications of such a Holistic understanding in terms of ethical human conduct, trustful and mutually fulfilling human behaviour and mutually enriching interaction with Nature.
4.	To analyze the value of harmonious relationship based on trust and respect in their life and profession

Course Outcomes (CO)

CO 1	Evaluate the significance of value inputs in formal education and start applying them in their life and profession
CO 2	Distinguish between values and skills, happiness and accumulation of physical facilities, the Self and the Body, Intention and Competence of an individual, etc.
CO 3	Examine the role of a human being in ensuring harmony in society and nature.
CO 4	Apply the understanding of ethical conduct to formulate the strategy for ethical life and profession.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	-	-	-	-	-	3	-	3	1	1	-	1
CO 2	-	-	-	-	-	3	-	3	1	1	-	1
CO 3	-	-	-	-	-	3	-	3	1	1	-	1
CO 4	-	-	-	-	-	3	-	3	1	1	-	1

UNIT-I

Introduction-Basic Human Aspiration, its fulfillment through All-encompassing Resolution: The basic human aspirations and their fulfillment through Right understanding and Resolution, Right understanding and Resolution as the activities of the Self, Self being central to Human Existence; All-encompassing Resolution for a Human Being, its details and solution of problems in the light of Resolution

UNIT-II

Understanding Human Being: Understanding the human being comprehensively as the first step and the core theme of this course; human being as co-existence of the self and the body; the activities and potentialities of the self; Basis for harmony/contradiction in the self

UNIT-III

Understanding Nature and Existence: A comprehensive understanding (knowledge) about the existence, Nature being included; the need and process of inner evolution (through self-exploration, self-awareness and self-evaluation), particularly awakening to activities of the Self: Realization, Understanding and Contemplation in the Self (Realization of Co-Existence, Understanding of Harmony in Nature and Contemplation of Participation of Human in this harmony/ order leading to comprehensive knowledge about the existence).

UNIT - IV

Understanding Human Conduct, All-encompassing Resolution & Holistic Way of Living: Understanding Human Conduct, different aspects of All-encompassing Resolution (understanding, wisdom, science etc.), Holistic way of living for Human Being with All-encompassing Resolution covering all four dimensions of human endeavor viz., realization, thought, behavior and work (participation in the larger order) leading to harmony at all levels from Self to Nature and entire Existence

Textbook(s):

1. R R Gaur, R Asthana, G P Bagaria, 2019 (2nd Revised Edition), A Foundation Course in Human Values and Professional Ethics. ISBN 978-93-87034-47-1, Excel Books, New Delhi.
2. Premvir Kapoor, Professional Ethics and Human Values, Khanna Book Publishing, New Delhi, 2022.

References:

1. Ivan Illich, 1974, Energy & Equity, The Trinity Press, Worcester, and Harper Collins, USA
2. E.F. Schumacher, 1973, Small is Beautiful: a study of economics as if people mattered, Blond & Briggs, Britain.
3. Sussan George, 1976, How the Other Half Dies, Penguin Press. Reprinted 1986.
4. Donella H. Meadows, Dennis L. Meadows, Jorgen Randers, William W. Behrens III, 1972, Limits to Growth – Club of Rome's report, Universe Books.
5. A Nagraj, 1998, Jeevan Vidya EkParichay, Divya Path Sansthan, Amarkantak.
6. P L Dhar, RR Gaur, 1990, Science and Humanism, Commonwealth Publishers.
7. A N Tripathy, 2003, Human Values, New Age International Publishers.
8. Subhas Palekar, 2000, How to practice Natural Farming, Pracheen (Vaidik) Krishi Tantra Shodh, Amravati.
9. E G Seebauer& Robert L. Berry, 2000, Fundamentals of Ethics for Scientists &Engineers, Oxford University Press
10. M Govindrajran, S Natrajan& V.S. Senthil Kumar, Engineering Ethics (including Human Values), Eastern Economy Edition, Prentice Hall of India Ltd.
11. B P Banerjee, 2005, Foundations of Ethics and Management, Excel Books.
12. B L Bajpai, 2004, Indian Ethos and Modern Management, New Royal Book Co., Lucknow. Reprinted 2008.

Embedded System Architecture and Design	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE	6	PCE	PCE-3	ECE-344T
CSE-in-EA	6	OAE-CSE-EA	OAE-1	ES-306T
EE-VDT	6	PC	PC	ES-306T
EC-ACT	6	OAE-ECE-EA	OAE-1	ES-306T
EAE	6	ES-EAE	ES-EAE-2B	ES-306T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To learn the architectural design of Embedded system.
2.	To understand the communication protocols in respect to advanced processors.
3.	Develop real time applications based on embedded systems.
4.	Apply embedded device based processing on RTOS.

Course Outcomes (CO)

CO 1	Ability to understand the architecture and features of microcontrollers 8051 and PIC.
CO 2	Ability to understand and apply the concepts of ARM processors and understand various Bus structures in programming.
CO 3	Ability to understand the concept of embedded software, RTOS and apply it in Embedded Programming.
CO 4	Ability to apply the knowledge of embedded operating systems to understand Mutli-Tasking, Scheduling and RTOS linux kernel.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	2	1	-	-	-	-	-	-	-	2	-	1
CO 2	2	1	-	-	-	-	-	-	-	2	-	2
CO 3	2	1	1	2	2	2	2	-	-	2	-	1
CO 4	-	1	1	2	2	2	2	-	-	2	-	1

UNIT I

Overview of Embedded Systems: Characteristics of Embedded Systems. Comparison of Embedded Systems with general purpose processors. General architecture and functioning of micro controllers. 8051 microcontrollers. PIC Microcontrollers: Architecture, Registers, memory interfacing, interrupts, Instructions, programming and peripherals.

UNIT II

ARM Processors: Comparison of ARM architecture with PIC micro controller, ARM 7 Data Path, Registers, Memory Organization, Instruction set, Programming, Exception programming, Interrupt Handling, Thumb mode Architecture. Bus structure: Time multiplexing, serial, parallel communication bus structure. Bus arbitration, DMA, PCI, AMBA, I2C and SPI Buses.

UNIT III

Embedded Software, Concept of Real Time Systems, Software Quality Measurement, and Compilers for Embedded System.

UNIT IV

RTOS: Embedded Operating Systems, Multi-Tasking, Multi-Threading, Real-time Operating Systems, RTLinux introduction, RTOS kernel, Real-Time Scheduling.

Textbook(s):

1. Design with PIC Microcontrollers, John B. Peatman, Pearson Education Asia, 2002.
2. ARM System Developer's Guide: Designing and Optimizing System Software, Andrew N. Sloss, Dominic Symes, Chris Wright, Morgan Kaufman Publication, 2004.
3. Computers as components: Principles of Embedded Computing System Design, Wayne Wolf, Morgan Kaufman Publication, 2000.

References:

1. The Design of Small-Scale embedded systems, Tim Wilmshurst, Palgrave 2003.
2. Embedded System Design, Mar wedel, Peter , Kluwer Publishers , 2004.

VHDL Programming	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ITE	6	PCE	PCE-1	CIE-326T
ECE	6	PCE	PCE-1	ECE-306T
EE-VDT	6	PC	PC	ECE-306T
CSE-in-EA	7	OAE-CSE-EA	OAE-2	ES-403T
EC-ACT	7	OAE-ECE-EA	OAE-2	ES-403T
EAE	7	ES-EAE	ES-EAE-3B	ES-403T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To provide knowledge of basics of VHDL Programming.
2.	To impart knowledge of Combinational logic circuit simulation and its implementation.
3.	To impart knowledge of simulation and implementation of Synchronous Sequential logic circuit.
4.	To impart knowledge of simulation and implementation of Asynchronous Sequential logic circuit.

Course Outcomes (CO)

CO 1	To understand the basics of VHDL Programming.
CO 2	To understand simulation and implementation of Combinational logic circuit.
CO 3	To understand simulation and implementation of Synchronous Sequential logic circuit.
CO 4	To understand simulation and implementation of Asynchronous Sequential logic circuit.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	2	2	3	3	2	2	2	-	1	2	2	3
CO 2	3	2	3	3	3	2	2	-	1	2	2	3
CO 3	3	2	3	3	3	2	2	-	1	2	2	3
CO 4	3	2	3	3	3	2	2	-	1	2	2	3

UNIT-I

Introduction to VHDL, design units, data objects, signal drivers, inertial and transport delays, delta delay, VHDL data types, concurrent and sequential statements, configuration declaration, instantiation.

UNIT-II

Combinational logic circuit design and VHDL implementation of following circuits –full adder, Subtractor, decoder, encoder, multiplexer, ALU, Subprograms – Functions, Procedures, attributes, generic, generate,

package, IEEE standard logic library, file I/O, test bench, barrel shifter, 4X4 key board encoder, multiplier, divider, Hamming code encoder and correction circuits.

UNIT-III

Sequential circuit design: flip-flops, registers, counters. **Synchronous Sequential circuit design:** finite state machines, Mealy and Moore, state assignments, design and VHDL implementation of FSMs, Linear feedback shift register (Pseudorandom and CRC).

UNIT – IV

Asynchronous sequential circuit design – primitive flow table, concept of race, critical race and hazards, design issues like metastability, synchronizers, clock skew and timing considerations Introduction to place & route process, Introduction to ROM, PLA, PAL, Architecture of CPLD and FPGA (Xilinx/Altera).

Textbook(s):

1. Stephen Brown, Zvonko Vranesic, "Fundamentals of Digital Logic with VHDL design", TMH.
2. Douglas Perry , "VHDL" 4th Edition, TMH.

References:

1. J. Bhasker, "A VHDL Primmer", Prentice Hall 1995.
2. Charles. H.Roth , "Digital System Design using VHDL", PWS (1998)
3. John F. Wakerley , "Digital Design Principles And Practices" , Pearson Education
4. Navabi Z , "VHDL-Analysis & Modelling of Digital Systems", McGraw Hill.
5. William I. Fletcher, "An Engineering Approach To Digital Design", Prentice Hall
6. M. Morris Mano, "Digital Design 3rd Edition", Pearson.

Semiconductor Devices and Modelling	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EE-VDT	6	PC	PC	VLSI-328T
EAE	6	VLSI-EAE	VLSI-EAE-1	VLSI-328T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To impart the basic operation of semiconductor devices.
2.	To impart the knowledge of semiconductor materials.
3.	To study the physics of junction device & its applications.
4.	To study FET structure & process simulation

Course Outcomes (CO)

CO 1	To understand the basic operation of semiconductor devices.
CO 2	To provide the knowledge of semiconductor materials.
CO 3	Understand the physics of junction device & its applications.
CO 4	Analyze FET structure & process simulation.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	2	3	3	3	2	2	-	2	2	3	3
CO 2	3	2	3	3	2	2	3	-	3	2	2	3
CO 3	3	3	3	2	3	2	3	-	2	2	3	2
CO 4	3	3	3	3	2	3	2	-	2	3	3	2

UNIT I

Review of semiconductor physics, p-n Junction diode: Physical operation, I-V characteristic and diode equation, Concept of load line, p-n junction capacitances (depletion and diffusion), small signal (low and high frequency) model, Large-signal model, Breakdown in p-n diodes, Zener diode, Poisson's equation.
Crystals and Band structures: Crystal Structure, Lattice, Lattice with basis, Band structure evolution, Density of states, Carrier Statistics.

UNIT II

Semiconductors in Equilibrium and Carrier Transport in Semiconductors: Semiconductor Materials, Concept of intrinsic and extrinsic semiconductors, Fermi level Carrier Concentration, Carrier Drift, Carrier Diffusion, Generation and Recombination Process, Continuity Equation, Thermionic Emission, Tunnelling, High Field Effects.

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UNIT III

Diode Applications: Rectifier circuits, Zener diode-based voltage regulators, limiting and clamping circuits, voltage multipliers, switching behaviour of p-n diode, SPICE model of p-n diode, an example of p-n diode data sheet., zener diode and LED, diode as a rectifier.
Physics of Junction Devices: Thermal Equilibrium Condition, Depletion Region, Depletion and Diffusion Capacitances, Current-Voltage Characteristics, Junction Breakdown, Metal Semiconductor Contacts, transistor (PNP and NPN) characteristics, current and voltage gain.

UNIT IV

FET: UJT, BJT, Introduction, channel transmission, Introduction to the Virtual source model, channel length modulation, drain induced barrier lowering, punch through, hot carrier effects, DC gate current, junction leakage: leakage currents, band to band tunnelling and GIDL.
Process Simulation /Process Modeling: Introduction of process simulation, modeling and simulation of oxidation and diffusion, Ion implantation, Masking, Fick's laws, Case Study: SUPERM.

Textbook(s):

1. Introduction to Semiconductor Materials and devices by M.S Tyagi, John Wiley & Sons, 5th Edition, 2005.
2. Semiconductor Devices: Modeling and Technology by A Dasgupta, N. Dasgupta, Prentice Hall, 2004.
3. Solid State Physics by Neil W. Ashcroft, N. David Mermin, Cengage Learning, 2011.

References:

1. Physics of Semiconductor Devices by S. M. Sze and Kwok K. Ng, John Wiley & Sons, 3rd Edition, 2002.
2. Solid State Electronic Devices by Ben G. Streetman and Sanjay Banerjee, Prentice Hall, 6th Edition 2005.
3. Semiconductor Device Fundamentals by Robert F. Pierret, Addison-Wesley Publishing, 1996.
4. Semiconductor Physics and Devices by Donald A. Neamen, McGrawHill, 3 rd Edition 2003.
5. Semiconductor Devices- Basic Principles by Jasprit Singh, John Wiley and Sons Inc., 2001.

VLSI	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EE/EEE	6	PCE	PCE-3	EEE-362T
EE-VDT	6	PC	PC	VLSI-330T
EAE	6	VLSI-EAE	VLSI-EAE-2	VLSI-330T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To understand the fundamental concepts of VLSI technology and design basic CMOS circuits for digital applications.
2.	To apply advanced VLSI design techniques including pipelining, memory design, low-power methodologies, and FPGA programming.
3.	To analyze and simulate complex VLSI circuits, including analog, mixed-signal, and high-frequency designs, considering noise, timing, and manufacturability challenges.
4.	To integrate VLSI components into complex systems, manage VLSI projects, and understand real-world applications and ethical considerations in VLSI technology.

Course Outcomes (CO)

CO 1	Understand the fundamental concepts of VLSI technology and design basic CMOS circuits for digital applications.
CO 2	Apply advanced VLSI design techniques including pipelining, memory design, low-power methodologies, and FPGA programming.
CO 3	Analyze and simulate complex VLSI circuits, including analog, mixed-signal, and high-frequency designs, considering noise, timing, and manufacturability challenges.
CO 4	Integrate VLSI components into complex systems, manage VLSI projects, and understand real-world applications and ethical considerations in VLSI technology.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	2	1	-	-	2	1	2	1
CO 2	3	3	3	3	2	1	-	-	2	1	2	1
CO 3	3	3	3	3	2	1	-	-	2	1	2	1
CO 4	3	3	3	3	2	1	-	-	2	1	2	1

Unit 1: VLSI Fundamentals and CMOS Technology

Introduction to VLSI Technology, MOS Transistor Theory and CMOS Logic Gates, Combinational Logic Design, Sequential Logic Design, ASIC Design Flow and Methodologies, VLSI Testing and Testability

Unit 2: Advanced VLSI Design Techniques

Pipelining and Parallel Processing in VLSI, Memory Design: SRAM and DRAM, Low Power VLSI Design Techniques, FPGA Architecture and Programming, High-Level Synthesis and System-Level Design.

Unit 3: VLSI Circuit Analysis and Simulation

Circuit Simulation Tools: SPICE, Cadence, Synopsys, Analog and Mixed-Signal VLSI Design, Noise Analysis in VLSI Circuits, Timing Analysis and Synchronization, RF and High-Frequency VLSI Design, Design for Manufacturability (DFM) and Yield Enhancement

Unit 4: VLSI System Integration

System-on-Chip (SoC) Design and Integration, VLSI Interconnects and Signal Integrity, VLSI Project Management and Documentation, Industry Practices and Case Studies, Ethical and Societal Implications of VLSI Technology.

Textbook:

1. Introduction to VLSI Circuits and Systems" by Jha, N. K., & Goswami, M. (2014).

References:

1. Weste, N. H. E., & Harris, D. M. (2011). CMOS VLSI Design: A Circuits and Systems Perspective. Pearson
2. Rabaey, J. M., Chandrakasan, A., & Nikolic, B. (2003). Digital Integrated Circuits: A Design Perspective. Pearson.
3. Brown, S., & Vranesic, Z. (2017). Fundamentals of Digital Logic with Verilog Design. McGraw-Hill Education.
4. Das, D. (2007). VLSI Design. McGraw-Hill Education.

Embedded System Architecture and Design Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE	6	PCE	PCE-3	ECE-344P
CSE-in-EA	6	OAE-CSE-EA	OAE-1	ES-306P
EE-VDT	6	PC	PC	ES-306P
EC-ACT	6	OAE-ECE-EA	OAE-1	ES-306P
EAE	6	ES-EAE	ES-EAE-2B	ES-306P

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Embedded System Architecture and Design) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Write a program to load three numbers into Accumulator and send them to port 1. (Keil)
2. Write an 8051 C program to send hex values for ASCII characters of 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D and E to port P1.
3. Write a program to configure watchdog timer in watchdog mode & interval mode.
4. Write an 8051 C program to get a byte of data form P1, wait ½ second (i.e., 500 ms) and then send it to P2.
5. Write an 8051 C Program to send the two messages “first name” and “last name” to the serial port. If SW = 0, send first name else if SW = 1, send last name. Set the baud rate at 9600, 8-bit data, and 1 stop bit.
6. Learn how to use Embest IDE for ARM and ARM Software Emulator.
7. Program to interface Stepper Motor to rotate the motor in clockwise and anticlockwise Directions.
8. Write a program to change ARM state mode by using MRS/MMSR instruction.
9. Write a random number generation function using assembly language.
10. Use assembly and C language to read/write words, half-words, bytes, half bytes from/to RAM.
11. Write programs that implement an interrupt service routine.
12. Write programs that use the RTC. Modify the setting of time and date. Display the current system clock time through the serial port.
13. Develop a project that accepts the keys of the keyboard pad through interrupt service routine and display the values on the 8-SEG LED.

VHDL Programming Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ITE	6	PCE	PCE-1	CIE-326P
ECE	6	PCE	PCE-1	ECE-306P
EE-VDT	6	PC	PC	ECE-306P
CSE-in-EA	7	OAE-CSE-EA	OAE-2	ES-403P
EC-ACT	7	OAE-ECE-EA	OAE-2	ES-403P
EAE	7	ES-EAE	ES-EAE-3B	ES-403P

Marking Scheme:

1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:

1. The course objectives and course outcomes are identical to that of (VHDL Programming) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Design all gates using VHDL.
2. Write VHDL programs for the following circuits, check the wave forms and the hardware generated

   i) half adder ii) full adder
3. Write VHDL programs for the following circuits, check the wave forms and the hardware generated

   i) multiplexer ii) demultiplexer
4. Write VHDL programs for the following circuits, check the wave forms and the hardware generated

   i) decoder ii) encoder
5. Write a VHDL program for a comparator and check the wave forms and the hardware generated
6. Write a VHDL program for a code converter and check the wave forms and the hardware generated
7. Write a VHDL program for a FLIP-FLOP and check the wave forms and the hardware generated
8. Write a VHDL program for a counter and check the wave forms and the hardware generated
9. Write VHDL programs for the following circuits, check the wave forms and the hardware generated

   i) ALU ii) shift register

Semiconductor Devices and Modelling Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EE-VDT	6	PC	PC	VLSI-328P
EAE	6	VLSI-EAE	VLSI-EAE-1	VLSI-328P

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Semiconductor Devices and Modelling) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis).
2. Measure, analyse, and model the IV characteristics of the diode
3. ZENER DIODE CHARACTERISTICS AND ZENER AS VOLTAGE REGULATOR
4. HALF -WAVE RECTIFIER WITH AND WITHOUT FILTER.
5. FULL -WAVE RECTIFIER WITH AND WITHOUT FILTER.
6. Draw the frequency response of CS amplifier using Multisim.
7. INPUT AND OUTPUT CHARACTERISTICS OF TRANSISTOR
8. Demonstrate the Volt-ampere characteristics of silicon-controlled rectifier.
9. To study the V-I characteristics of FET.
10. To study the equivalent circuit model for MOSFET.
11. To study FET model for calculating Drain Induced Barrier Lowering (DIBL).
12. To study FET model for calculating Gate induced drain leakage (GIDL).

VLSI Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EE/EEE	6	PCE	PCE-3	EEE-362P
EE-VDT	6	PC	PC	VLSI-330P
EAE	6	VLSI-EAE	VLSI-EAE-2	VLSI-330P

Marking Scheme:

1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:

1. The course objectives and course outcomes are identical to that of (VLSI) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To study the MOS characteristics and introduction to tanner EDA software tools.
2. To design and study the DC characteristics of PMOS and NMOS EDA software tools.
3. To design and study the DC and AC characteristics of resistive load inverter EDA software tools.
4. To design and study the DC and AC characteristics of CMOS inverter EDA software tools.
5. To design and study the characteristics of CMOS NAND and NOR gate EDA software tools.
6. To design any Boolean function using transmission gates EDA software tools.
7. To design and study the characteristics of CMOS multiplexer EDA software tools.
8. To design and study the characteristics of D latch EDA software tools.
9. To design and study the characteristics of Full adder EDA software tools.
10. To design and study the layout of PMOS and NMOS transistors EDA software tools.
11. To design and study the layout of CMOS inverter EDA software tools.

Principles of Entrepreneurship Mindset	L	P	C
	2		2

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
All	7	HS/MS	MS	MS-401

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To understand basic aspects of establishing a business in a competitive environment
2.	To apply the basic understanding to examine the existing business ventures
3.	To examine various business considerations such as marketing, financial and teaming etc.
4.	To assess strategies for planning a business venture

Course Outcomes (CO)

CO 1	Understand basic aspects of establishing a business in a competitive environment
CO 2	Apply the basic understanding to examine the existing business ventures
CO 3	Examine various business considerations such as marketing, financial and teaming etc.
CO 4	Assessing strategies for planning a business venture

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	2	2	1	2	-	2	-	-	1	2	3	2
CO 2	2	2	1	2	-	2	-	-	1	2	3	2
CO 3	2	2	1	2	-	2	-	-	1	2	3	2
CO 4	2	2	1	2	-	2	-	-	1	2	3	2

UNIT-I

Entrepreneurial perspective: Foundation, Nature and development ofentrepreneurship, importance of entrepreneurs,Entrepreneurial Mind, Individual entrepreneur Typesof entrepreneurs, Entrepreneurship in India

UNIT-II

Beginning Considerations: Creativity and developing business ideas; Creatingand starting the venture; Building a competitiveadvantage; Opportunity recognition, Opportunityassessment; Legal issues

UNIT-III

Developing Financial Plans: Sources of Funds,Managing Cash Flow,Creating a successful Financial PlanDeveloping a business plan

UNIT - IV

Developing Marketing Plans: Developing a powerful Marketing Plan, E-commerce,Integrated Marketing Communications
Leading Considerations: Developing Team, Inviting candidates to join team,Leadership model

Textbook(s):

1. Robert D Hisrich, Michael P Peters & Dean A Shepherd, "Entrepreneurship" 10th Edition,McGraw Hill Education, 2018

References:

1. Norman M. Scarborough and Jeffery R. cornwell, "Essentials of entrepreneurship and small business management" 8th Edition, Pearson, 2016
2. Rajiv Roy, "Entrepreneurship", 2nd Edition, Oxford University Press, 2011
3. Sangeeta Sharma, "Entrepreneurship Development", 1st Edition, Prentice-Hall India, 2016
4. John Mullins, "The New Business Road Test: What entrepreneurs and investors should dobefore launching a lean start-up" 5th Edition, Pearson Education, 2017
5. Charantimath, Entrepreneurship Development and Small Business Enterprise, Pearson Education.

CMOS Analog Integrated Circuit Design	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE	6	PCE	PCE-3	ECE-338T
EE-VDT	7	PC	PC	VLSI-443T
EAE	7	VLSI-EAE	VLSI-EAE-3	VLSI-443T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To impart the knowledge of basic MOS device Physics, low and high frequency analog MOSFET modelling.
2.	To provide the concepts of Single Stage and Differential amplifiers and their analysis.
3.	To provide the concepts of active and passive current mirrors, large signal analysis, small signal analysis and frequency response of amplifiers.
4.	To provide the concepts of feedback circuits, their topologies, operational amplifier and oscillators.

Course Outcomes (CO)

CO 1	To understand the basics of MOS device and its low and high frequency modelling.
CO 2	To understand the concepts of Single Stage and Differential amplifiers and their analysis
CO 3	To understand the concepts current mirrors, large signal analysis, small signal analysis and frequency response of amplifiers.
CO 4	To understand the concepts of feedback circuits, their topologies, operational amplifier and oscillators

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	2	2	3	3	2	2	2	-	1	2	2	3
CO 2	3	2	3	3	3	2	2	-	1	2	2	3
CO 3	3	2	3	3	3	2	2	-	1	2	2	3
CO 4	3	2	3	3	3	2	2	-	1	2	2	3

UNIT-I

Introduction: Analog integrated circuit design, Circuit design consideration for MOS challenges in analog circuit design, Recent trends in analog VLSI circuits.

Basic MOS Device Physics. Analog MOSFET modeling: MOS transistor, Low frequency MOSFET model, High frequency MOSFET model, temperature effect in MOSFET and Noise in MOSFET.

UNIT-II

Single Stage Amplifier: Basic concept, Introduction to CS, CD, CG Amplifiers, analysis of CS amplifier with (resistive load, diode connected load, current source load, triode load, source degeneration), Analysis of Source Follower (CD amplifier), analysis of CG amplifier, analysis of cascode stage and folded cascode.
Differential amplifiers: Single ended and differential operation, basic differential pair, common mode response.

UNIT-III

Passive and active current mirrors: Basic current mirrors, cascade current mirrors, active current mirrors; large signal analysis, small signal analysis, common mode properties.
Frequency Response of amplifiers: General consideration: Association of Poles with Nodes, Miller Effect and Miller's Theorem and its dual Frequency Response of CS stage, source follower, common gate stage, cascade stage. Frequency Response of Differential Amplifier ,

UNIT - IV

Feedback: Properties of Feedback Circuits, Feedback Topologies.
Operational amplifier: one-stage and two- stage Op Amps, gain boosting, comparison, Common-Mode Feedback, Input Range Limitations, Slew Rate. Bandgap references, **Oscillators:** Ring oscillator, LC oscillator, voltage controlled oscillator.

Textbook(s):
1. Design of Analog CMOS Integrated Circuits" by Behzad Razavi; Tata McGraw-Hill.
2. CMOS analog Circuit Design by Allen Holberg, Oxford University Press.

References:
1. Analog Integrated Circuit Design by David A. Johns and Ken Martin John Wiley & Son.
2. R. J. Baker, H. W. Li, and D. E. Boyce , " CMOS circuit design, layout, and simulation", Wiley-IEEE Press,2007.

CMOS Digital Circuits Design	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EE-VDT	7	PC	PC	VLSI-445T
EAE	7	VLSI-EAE	VLSI-EAE-4	VLSI-445T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To provide the concepts of VLSI Design flow, basics of MOS device, CMOS Inverter, Circuit Characterization and Performance Estimation, BiCMOS logic.
2.	To provide the concepts of Switching characteristics, Clocking Strategies, combinational and Clocked sequential circuits.
3.	To provide the concepts of Subsystem designing and Semiconductor Memories.
4.	To provide the concepts of FSM, digital phase-locked loop (DPLL), adiabatic logic circuits and Field Programmable Devices.

Course Outcomes (CO)

CO 1	To understand the concepts of VLSI Design flow, basics of MOS device, CMOS Inverter, Circuit Characterization and Performance Estimation, BiCMOS logic.
CO 2	To understand the concepts of Switching characteristics, Clocking Strategies, combinational and Clocked sequential circuits.
CO 3	To understand the concepts of Subsystem designing and Semiconductor Memories.
CO 4	To understand the concepts of FSM, digital phase-locked loop (DPLL), adiabatic logic circuits and Field Programmable Devices.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	2	2	3	2	3	2	2	-	1	2	2	2
CO 2	2	2	3	3	3	2	2	-	1	2	2	3
CO 3	2	2	3	3	3	2	2	-	1	2	2	3
CO 4	2	2	3	3	3	2	2	-	1	2	2	3

UNIT-I

VLSI Design flow, Design Hierarchy, Regularity, Modularity and Locality. VLSI design styles, Design quality, Packaging technology. MOS device design equations, second order effects, the complementary CMOS Inverter DC characteristics, Circuit Characterization and Performance Estimation: Parasitic effect in Integrated Circuits, Resistance estimation. Capacitance estimation, Inductance. BiCMOS logic gates, super-buffers.

UNIT-II

Switching characteristics, CMOS - Gate transistor sizing. Power dissipation, CMOS Logic Structures, Clocking Strategies, CMOS Process Enhancement & Layout Considerations: Interconnect circuit elements. Stick diagram, Layout design rules, Latch up, Technology related CAD issues. Multiplexer, code converters.
Clocked sequential circuits-two phase clocking, charge storage, dynamic register element, dynamic shift register.

UNIT-III

Subsystem design: Subsystem design process, Design of ALU subsystem, Adders, Multipliers, barrel and logarithmic shifters.
Semiconductor Memories: Dynamic Random Access Memories (DRAM), Static RAM, non-volatile memories, flash memories, low-power memory.

UNIT – IV

Finite State Machine (FSM), digital phase-locked loop (DPLL), adiabatic logic circuits
Field Programmable Devices: Definitions of Relevant Terminology, Evolution of Programmable Logic Devices, User-Programmable Switch Technologies. Computer Aided Design (CAD) Flow for FPDs, Programmable Logic, Programmable Logic Structures, Programmable Interconnect. Reprogrammable Gate Array, Commercially Available SPLDs, CPLDs and FPGAs, Gate Array Design, Sea-of-Gates.

Textbook(s):

1. Design of Analog CMOS Integrated Circuits" by Behzad Razavi; Tata McGraw-Hill.
2. CMOS analog Circuit Design by Allen Holberg, Oxford University Press.
3. Introduction to VLSI Circuits and Systems, John P. Uyemura John Wiley & Sons.

References:

1. Analog Integrated Circuit Design by David A. Johns and Ken Martin John Wiley & Son.
2. R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout, and simulation", Wiley-IEEE Press,2007.

Low Power VLSI Design	L	P	C
	3		3

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE	7	PCE	PCE-5	ECE-419T
EE-VDT	7	PC	PC	VLSI-449T
EAE	7	VLSI-EAE	VLSI-EAE-5B	VLSI-449T

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To impart the basic principles of low power VLSI design and its need.
2.	To impart the knowledge of low power architecture and various low power design approaches.
3.	To impart the knowledge of different type of low power techniques and low voltage low power adders.
4.	To impart the knowledge of low voltage low power memories in VLSI design.

Course Outcomes (CO)

CO 1	To understand the basic principles of low power VLSI design and its need.
CO 2	To study the low power architecture and various low power design approaches.
CO 3	To provide the knowledge of different type of low power techniques and low voltage low power adders.
CO 4	Understand low voltage low power memories in VLSI design.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	3	3	3	3	3	3	-	2	2	2	3
CO 2	3	3	3	3	3	3	2	-	2	1	2	3
CO 3	3	3	3	3	3	3	2	-	2	1	2	3
CO 4	3	3	3	3	3	2	2	-	2	1	2	2

UNIT I

Introduction to low power VLSI design an overview, Need for low power, low power design Limitations, power supply voltage, Power and Energy basics, Sources of power dissipation-Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects – Drain Induced Barrier Lowering, Gate Induced Drain leakage and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect, threshold voltage, scaling, interconnect wires. CMOS leakage current, static current, basic principles of low power design, probabilistic power analysis, random logic signal-probability and frequency-power analysis techniques.

UNIT II

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits. To study basics of CMOS. Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, and Mask level Measures, capacitive power estimation, static state power, gate level capacitance estimation.

UNIT III

Low Power Techniques: Circuit level: Power consumption in circuits. Dynamic Power Optimization: multiple supply voltages, transistor sizing, and Static power Optimization: Multiple thresholds transistor, Flip Flops and Latches design, high capacitance nodes, and low power digital cells library.
Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures Ripple Carry Adders, Carry Look- Ahead Adders, Carry Select Adders, Carry Save Adders.

UNIT IV

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbook(s):

1. Low Power Design Methodologies by J. M. Rabaey, M.Pedram.
2. Low-Power CMOS VLSI Circuit Design by K. Roy and S. C.Prasad.

References:

1. Practical Low Power Digital VLSI Design by Gary K. Yeap, KAP, 2002.
2. Digital Integrated Circuits: A Design Perspective, Second Edition by J. M. Rabaey, A. P. Chandrakasan and B. Nikolic, Pearson.
3. Low-Power CMOS Design, P. Chandrakasan and RW Broderson, IEEE Press.

VLSI Testing	L	P	C
	4		4

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EE-VDT	7	PC	PC	VLSI-451
EAE	7	VLSI-EAE	VLSI-EAE-5C	VLSI-451

Marking Scheme:

1. Teachers Continuous Evaluation: 25 marks
2. Term end Theory Examinations: 75 marks

Instructions for paper setter:

1. There should be 9 questions in the term end examinations question paper.
2. The first (1st) question should be compulsory and cover the entire syllabus. This question should be objective, single line answers or short answer type question of total 15 marks.
3. Apart from question 1 which is compulsory, rest of the paper shall consist of 4 units as per the syllabus. Every unit shall have two questions covering the corresponding unit of the syllabus. However, the student shall be asked to attempt only one of the two questions in the unit. Individual questions may contain upto 5 sub-parts / sub-questions. Each Unit shall have a marks weightage of 15.
4. The questions are to be framed keeping in view the learning outcomes of the course / paper. The standard / level of the questions to be asked should be at the level of the prescribed textbook.
5. The requirement of (scientific) calculators / log-tables / data – tables may be specified if required.

Course Objectives :

1.	To enhance knowledge of the fault modeling in VLSI circuits.
2.	To create vectors to test a circuit efficiently covering maximum faults.
3.	Learn about application in modern digital design
4.	Use modern CAD tools for VLSI testing and verification.

Course Outcomes (CO)

CO 1	To understand fault modelling in VLSI circuits.
CO 2	To create vectors for test a circuit efficiently covering maximum faults.
CO 3	Understanding the application in modern digital design
CO 4	Using modern CAD tools for VLSI testing and verification.

Course Outcomes (CO) to Programme Outcomes (PO) mapping (scale 1: low, 2: Medium, 3: High)

	PO01	PO02	PO03	PO04	PO05	PO06	PO07	PO08	PO09	PO10	PO11	PO12
CO 1	3	2	3	2	3	2	1	-	2	1	1	1
CO 2	3	2	3	2	3	1	1	-	2	1	-	1
CO 3	3	2	3	2	2	2	1	-	2	1	2	2
CO 4	3	3	3	2	3	2	1	-	2	1	2	2

UNIT I

Physical fault sandtheir modelling. Fault equivalence and dominance, fault collapsing, Fault simulation: parallel, deductive and concurrent techniques; critical path-tracing. Test generation for combinational circuits: Boolean differenced-algorithm, Podem, random etc.

UNIT II

Exhaustive, random and weighted test pattern generation, aliasing and its effect on fault coverage. PLA testing: cross-point fault model, test generation, easily testable designs. Memory testing: permanent, intermittent and pattern-sensitive faults; test generation. Delay faults and hazards; test pattern generation techniques, ATPG and its different types.

UNIT III

Test pattern generation for sequential circuits: ad-hoc and structures techniques scan path and LSSD, boundary scan. Built-in self-test techniques: LBIST and MBIST. Verification: logic level (combinational and sequential circuits), RTL-level (data path and control path).

UNIT IV

Verification of embedded systems. Use of formal techniques: decision diagrams, logic-based approaches. ASIC/IP Verification, direct and random testing, Error detection and correction codes.

Textbook(s):

1. Essentials of Electronic Testing, M. L. Bushnell and V. D. Agrawal,3rd Kluwer Academic Publishers 2002.
2. Delay Fault Testing for VLSI Circuits, A. Krstic and K-T Cheng,3rd Kluwer Academic Publishers. 2003.
3. Testing of Digital Systems, N. K. Jha and S. Gupta, 2nd, Cambridge University Press. 2003.

References:

1. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, 3rd, Wiley-IEEE Press. 1994
2. B Fault Tolerant and Fault Testable P. K. Lala, 4th, Hardware Design, Prentice-Hall. 1986.

CMOS Analog Integrated Circuit Design Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE	6	PCE	PCE-3	ECE-338P
EE-VDT	7	PC	PC	VLSI-443P
EAE	7	VLSI-EAE	VLSI-EAE-3	VLSI-443P

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (CMOS Analog Integrated Circuit Design) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. Introduction to Cadence Virtuoso full custom design flow.
2. To design and study the Characteristics of MOS transistors.
3. To design and study inverter in CMOS configuration..
4. To study and design CS amplifier using resistive load and diode connected load.
5. To study and design CS amplifier using current source load and triode load.
6. To study and design CS amplifier as source degeneration.
7. To design and analyze source follower (Common Drain) amplifier.
8. To design and analyze Common Gate amplifier.
9. To design and analyze Cascode amplifier using ideal current source and PMOS current source.
10. To design and analyze Basic current mirror and Cascode current mirror.
11. To design and analyze differential amplifier using current mirror.
12. To design and analyze Ring Oscillator circuit.

CMOS Digital Circuits Design Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
EE-VDT	7	PC	PC	VLSI-445P
EAE	7	VLSI-EAE	VLSI-EAE-4	VLSI-445P

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (CMOS Digital Circuits Design) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

1. To study the MOS characteristics and introduction to tanner EDA software tools.
2. To design and study the transient and DC characteristics of CMOS inverter.
3. To design and study ALU.
4. To design and study the characteristics of CMOS Full adder.
5. To design and study the characteristics of CMOS multiplexer.
6. To design and study the code converters.
7. To design any Boolean function using transmission gates.
8. To design and study the transient characteristics of CMOS XOR/XNOR.
9. To design and study the characteristics of Multiplier circuit.
10. To design and study the characteristics of CMOS D- Flip Flop.
11. To design and study the characteristics of CMOS J-K Flip Flop.
12. To design study 3- bit counter.

Low Power VLSI Design Lab	L	P	C
		2	1

Discipline(s) / EAE / OAE	Semester	Group	Sub-group	Paper Code
ECE	7	PCE	PCE-5	ECE-419P
EE-VDT	7	PC	PC	VLSI-449P
EAE	7	VLSI-EAE	VLSI-EAE-5B	VLSI-449P

Marking Scheme:
1. Teachers Continuous Evaluation: 40 marks
2. Term end Theory Examinations: 60 marks

Instructions:
1. The course objectives and course outcomes are identical to that of (Low Power VLSI Design) as this is the practical component of the corresponding theory paper.
2. The practical list shall be notified by the teacher in the first week of the class commencement under intimation to the office of the Head of Department / Institution in which the paper is being offered from the list of practicals below. Atleast 10 experiments must be performed by the students, they may be asked to do more. Atleast 5 experiments must be from the given list.

Note: Experiments shall be carried out using Tanner/Mentor Graphics/Cadence

1. Introduction to SPICE (Operating Point Analysis, DC Sweep, Transient Analysis, AC Sweep, Parametric Sweep, Transfer Function Analysis)
2. Study the equivalent circuit model for MOS Transistor.
3. I-V Curves of NMOS and PMOS Transistors.
4. DC Characteristics of CMOS Inverters (VTC, Noise Margin).
5. Dynamic Characteristics of CMOS Inverters (Propagation Delay, Power Dissipation).
6. Schematic Entry/Simulation/ Layout of CMOS Combinational Circuits.
7. To study FET model for calculating Drain Induced Barrier Lowering (DIBL).
8. To study FET model for calculating Gate induced drain leakage (GIDL).
9. CMOS Static / Dynamic logic circuit (register cell).
10. CMOS Latch.
11. Flip Flops.
12. Adders: Ripple Carry Adders, Carry Look- Ahead Adders
13. Memories and State Machines: Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Arithmetic Multipliers using FSMs.